APPENDIX A

Register Structure

This appendix gives a brief description of the CAN controller registers. For more detailed information, please refer to the *Stand-alone CAN-controller Data Book* from Philips Semiconductors Microcontroller Products. (You may also find the information on the enclosed disk under the "Manual" directory, in the Word 6.0 file: REGISTER.DOC.)

CAN controller address allocation

Philips PCX82C200 CAN controller

ADDRESS

0	CONTROL	control segment
1	COMMAND	
2	STATUS	
3	INTERRUPT	
4	ACCEPTANCE CODE	
5	ACCEPTANCE MASK	
6	BUS TIMING 0	
7	BUS TIMING 1	
8	OUTPUT CONTROL	
9	TEST	

10	IDENTIFIER	descriptor	transmit buffer
11	RTR BIT, DATA LENGTH CODE		
12	BYTE 1	data field	
13	BYTE 2		
14	BYTE 3		
15	BYTE 4		
16	BYTE 5		
17	BYTE 6		
18	BYTE 7		
19	BYTE 8		

20	IDENTIFIER	descriptor	receive buffers
21	RTR BIT, DATA LENGTH CODE		
22	BYTE 1	data field	
23	BYTE 2		
24	BYTE 3		
25	BYTE 4		
26	BYTE 5		
27	BYTE 6		
28	BYTE 7		
29	BYTE 8		

Register address map

#	TITLE	ADDR	7	6	5	4	3	2	1	0
Control Segment										
1	Control Register	0	Test Mode	Sync	Reserv	Overru Interr Enable	Error Interrup Enable	Transm Interr Enable	Receive Interrup Enable	Reset Request
2	Command Register	1	Reserv	Reserv	Reserv	Goto Sleep	Clear Overrun Status	Releas Receiv Buffer	Abort Transmis	Transmis Request
3	Status Register	2	Bus Status	Error Status	Transm Status	Receiv Status	Transmis Complete Status	Transm Buffer Access	Data Overrun	Receive Buffer Status
4	Interrup Register	3	Reserv	Reserv	Reserv	Wake-U Interr	Overrun Interrup	Error Interr	Transmit Interrup	Receive Interrup
5	Acceptan Code Register	4	AC.7	AC.6	AC.5	AC.4	AC.3	AC.2	AC.1	AC.0
6	Acceptan Mask Register	5	AM.7	AM.6	AM.5	AM.4	AM.3	AM.2	AM.1	AM.0
7	Bus Timing Register 0	6	SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0
8	Bus Timing Register 1	7	SAM	TSEG2.	TSEG2.	TSEG2.	TSEG1.3	TSEG1.	TSEG1.1	TSEG1.0
9	Output Control Register	8	OCTP1	OCTN1	OCPOL1	OCTP0	OCTN0	OCPOL0	OCMODE1	OCMODE0
10	Test Register (note 1)	9	Reserv	Reserv	Map Intern Regist	Connec RX Buffer 0 CPU	Connect TX Buffer CPU	Access Intern Bus	Normal RAM Conncet	Float Output Driver
Transmit Buffer										
11	Identifi	10	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
	RTR, Data Length	11	ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0

Register descriptions

Control Register (CR)

The Control Register is used to change the behavior of the PCX82C200. Control bits may be set or reset by the attatched micro-controller, which uses the Control Register as a read/write memory.

Command Register (CMR)

A command bit initiates an action within the transfer layer of the PCX82C200. If a read access is perfomed to this address, the byte 11111111 (binary) is returned.

Status Register (SR)

The Status Register reflects the status of the PCX82C200 bus controller. The Status Register appears to the microcontroller as a read-only memory.

Interrupt Register (IR)

The Interrupt Register allows identification of an interrupt source. When one or more of this register's bits are set, the INT pin is activated. All bits are reset by the PCX82C200 after this register is read by the microcontroller. This register appears to the microcontoller as a read-only memory.

Acceptance Code Register (ACR)

The Acceptance Code Register is part of the acceptance filter of the PCX82C200. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present). When a message which passes the acceptance test is received and if there is an empty Receive Buffer, then the respective Descriptor and Data Field are sequentially stored in this empty buffer. In the case that there is no empty Receive Buffer, the Data Overrun bit is set HIGH (overrun).

Acceptance Mask Register (AMR)

The Acceptance Mask Register is part of the acceptance filter of the PCX82C200. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present). The Acceptance Mask Register classifies the corresponding bits of the acceptance code as "relevant" or "don't care" for acceptance filtering.

Bus Timing Register 0 (BTR0)

The Bus Timing Register 0 defines the values of the Baud Rate Prescaler (BRP) and the Synchronization Jump Width (SJW). This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).

Bus Timing Register 1 (BTR1)

The Bus Timing Register 1 defines the length of the bit period, the location of the sample point, and the number of samples to be taken at each sample point. This register can be accessed (read/write) if the Reset Request bit is set HIGH (present).

Output Control Register (OCR)

The Output Control Register allows, under software control, the setup of different driver configurations. This register may be accessed (read/write) if the Reset Request bit is set HIGH (present).

Test Register (TR)

The Test Register is used only for production testing.

Transmit Buffer

The Transmit Buffer stores a message from the microcontroller to be transmitted by the PCX82C200. It is subdivided into the Descriptor and Data Field. The Transmit Buffer can be written to and read from by the microcontroller.

Receive Buffer

The layout of the Receive Buffer and the individual bytes correspond to the definitions given for the Transmit Buffer layout, except that the addresses start at 20 instead of 10.