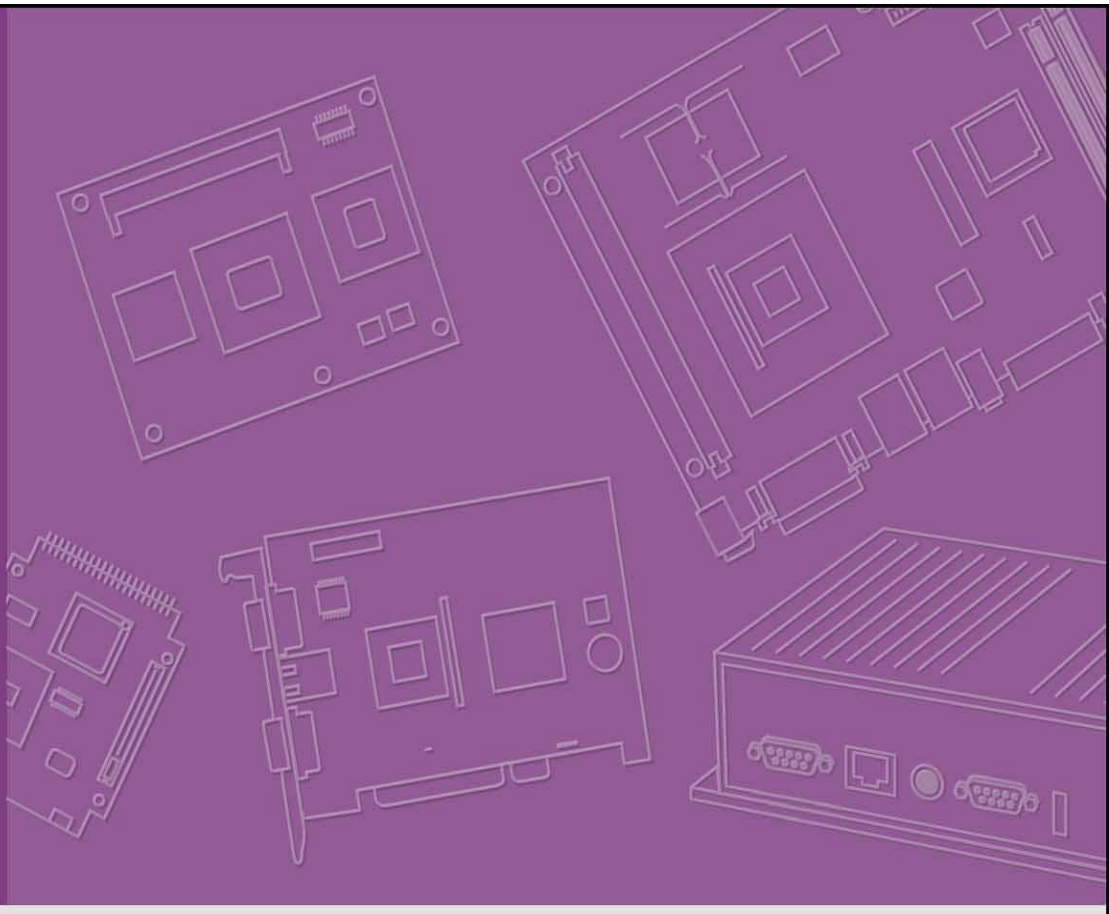
Embedded - IoT

CarrierBoard
Design Guide



COM Express®

SOM-5992 COMe TYPE7

R1210 2018’09’25

ADVANTECH
Enabling an Intelligent Planet

Contents

List of Tables

List of Figures

1 Introduction

1.1 About This Document

This design guide provides information for designing a custom system Carrier Board for COM Express Type 7 Module. It includes Signal Descriptions, Routing Guidelines and Trace Length Guidelines. The main purpose is designing Carrier Board for helping customers fast and easy using the module of Advantech to be designed.

1.2 Acronyms / Definitions

Table 1: Acronyms / Definitions Signal Table Terminology Descriptions

Term	*Description*
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3V3_SBY	Bi-directional 3.3V tolerant active during Suspend and running state.
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power input/output
S0, S1, S2, S3, S4, S5	System states describing the power and activity level S0 Full power, all devices powered S1 S2 S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
10GBase-KR	10 Gbit internal copper interface. Operates over a single lane and uses the same physical layer coding (defined in IEEE 802.3 Clause 49) as 10GBASE-LR (Single Mode Fiber 1310 nm) /ER (Single Mode Fiber 1550 nm) /SR (Multi Mode Fiber 850 nm)
10GBase-KX4	4x 10 Gbit internal copper interface. Operates over four lanes and uses the same physical layer coding (defined in IEEE 802.3 Clause 48) as 10GBASE-CX4
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems

Term	*Description*
Basic Module	COM Express 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
BMC	Baseboard Management Controller
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer.
Carrier Board	An application specific circuit board that accepts a COM Express Module.
Compact Module	COM Express 95x95 Module form factor
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
EAPI	Embedded Application Programming Interface Software interface for COM Express specific industrial functions • System information • Watchdog timer • I2C Bus • Flat Panel brightness control • User storage area • GPIO
EEPROM	Electrically Erasable Programmable Read-Only Memory
eSPI	Enhanced Serial Peripheral Interface
Extended Module	COM Express 155mm x 110mm Module form factor.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
Gb	Gigabit
GBE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
LAN	Local Area Network
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.

Term	*Description*
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LS	Least Significant
MDIO	Management Data Input/Output, or MDIO, is a 2-wire serial bus that is used to manage PHYs or physical layer devices in media access controllers (MACs).
ME	Management Engine
Mini Module	COM Express 84x55mm Module form factor
MS	Most Significant
NA	Not Available
NC	No Connect
NC-SI	Network Controller Sideband Interface
OEM	Original Equipment Manufacturer
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s
PCB	Printed Circuit Board
PCI Express PCIE	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of seven COM Express definitions for the signals that appear on the COM Express Module connector pins.
Ra	Roughness Average – a measure of surface roughness, expressed in units of length.
ROM	Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SAFS	eSPI tTerm for Slave Attached Flash Sharing where the Flash component is attached behind a BMC component.
SATA	Serial AT Attachment: serial-interface standard for hard disks
SCSI	Small Computer System Interface – an interface standard for high end disk drives and other computer peripherals

Terminology	*Description*
SDP	Software-Definable Pin
SGMII	Serial Gigabit Media Independent Interface
SM Bus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
SPI	Serial Peripheral Interface
Super I/O	An integrated circuit, typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface.
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
USB	Universal Serial Bus
WDT	Watch Dog Timer.
XAUI	10 Gigabit / sec Attachment Unit Interface.
XGMII	10 Gigabit Media Independent Interface

1.3 Reference Documents

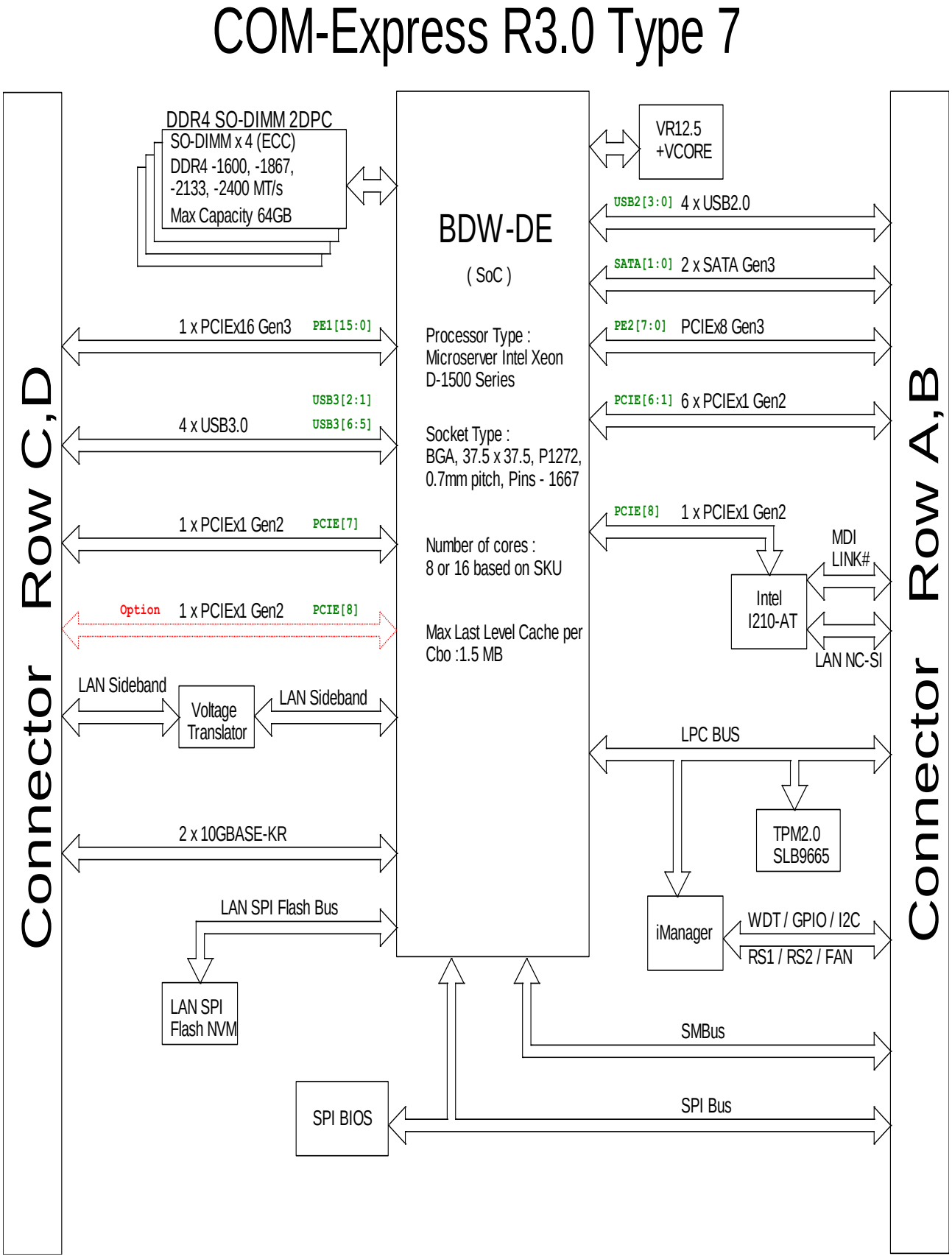
Document
PICMGR COM.0 Revision 3.0 COM Express Base Specification, 2017’03’31 Final
Intel EDS Document
Intel Layout Guide Document
ATX12V Power Supply Design Guide Rev. 2.01

1.4 Revision History

Revision	Date	PCB Rev.	Changes
0.10	2017’02’14	A101-1	
1.00	2017’10’02	A101-2	1. Change NC-SI interface connection from 10G to GbE0 & add GbE0 SDP Pin connection to B2B Conn. 2. Remove 10GB NC-SI connection to B2B Conn.
1.10	2018’03’02	A101-2	1. Modify AC coupling cap of the PCIe BUS.
1.20	09 25, 2018	A101-2	1. Modify LPC Clock output to 24MHz.

1.5 SOM-5992 Block Diagram

Figure 1: SOM-5992 Block Diagram



1.6 Module Pin-out Types 7 - Required and Optional Features

COM Express Required and Optional features are summarized in the following table. The features identified as Minimum (Min.) ***shall*** be implemented by all Modules. Features identified up to Maximum (Max) ***may*** be additionally implemented by a Module.

Table 2: Module Pin-out - Required and Optional Features

Feature	Type 7 Min / Max	SOM-5992
System I/O		
PCI Express Lanes 0 - 5	6 / 6	6
PCI Express Lanes 6 - 15	0 / 10	10
PCI Express Lanes 16 - 31	0 / 16	16
10G LAN Ports 0 - 3	0 / 4	2
NC-SI	0 / 1	1
1Gb LAN Port 0	1 / 1	1
Serial Ports 1 - 2	0 / 2	2
CAN interface on SER1	0 / 1	0
SATA Ports	0 / 2	2
USB 2.0 Ports	4 / 4	4
USB0 Client	0 / 1	0
USB 3.0 Ports	0 / 4	4
LPC Bus or eSPI	1 / 1	1
SPI (Devices)	1 / 2	2
Rapid Shutdown	0 / 1	0
System Management		
SDIO (muxed on GPIO)	0 / 1	0
General Purpose I/O	8 / 8	8
SMBus	1 / 1	1
I2C	1 / 1	1
Watchdog Timer	0 / 1	1
Speaker Out	1 / 1	1
Carrier Board BIOS Flash Support	0 / 1	1
Reset Functions	1 / 1	1
Trusted Platform Module	0 / 1	1
Power Management		
Thermal Protection	0 / 1	1
Battery Low Alarm	0 / 1	1
Suspend/Wake Signals	0 / 3	2
Power Button Support	1 / 1	1

Feature	Type 7 Min / Max	SOM-5992
Power Good	1 / 1	1
VCC_5V_SBY Contacts	4 / 4	4
Sleep Input	0 / 1	1
Lid Input	0 / 1	1
Carrier Board Fan Control	0 / 1	1
Power		
VCC_12V Contacts	24 / 24	24

2 COM Express Type 7 Interfaces

2.1 COM Express Type 7 Connector Layout

Figure 2: COM Express Type7 Connector Layout

NA

2.2 COM Express Type 7 Connector Pin-out

Table 3: COM Express Type 7 Pin-out

Connector Rows A and B

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
A1	GND(FIXED)		B1	GND(FIXED)	
A2	GBE0_MDI3-		B2	GBE0_ACT#	
A3	GBE0_MDI3+		B3	LPC_FRAME#/ESPI_CS0#	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0/ESPI_CS0	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1/ESPI_CS1	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2/ESPI_CS2	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3/ESPI_CS3	LPC_AD3
A8	GBE0_LINK#		B8	LPC_DRQ0#/ESPI_ALERT0#	LPC_DRQ0#
A9	GBE0_MDI1-		B9	LPC_DRQ1#/ESPI_ALERT1#	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK/ESPI_CK	LPC_CLK
A11	GND(FIXED)		B11	GND(FIXED)	
A12	GBE0_MDI0-		B12	PWRBTN#	
A13	GBE0_MDI0+		B13	SMB_CK	
A14	GBE0_CTREF	NC	B14	SMB_DAT	
A15	SUS_S3#		B15	SMB_ALERT#	
A16	SATA0_TX+		B16	SATA1_TX+	
A17	SATA0_TX		B17	SATA1_TX	
A18	SUS_S4#		B18	SUS_STAT#/ESPI_RESET#	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+	
A20	SATA0_RX		B20	SATA1_RX-	
A21	GND(FIXED)		B21	GND(FIXED)	
A22	PCIE_TX15+		B22	PCIE_RX15+	
A23	PCIE_TX15-		B23	PCIE_RX15-	
A24	SUS_S5#	SUS_S4#	B24	PWR_OK	
A25	PCIE_TX14+		B25	PCIE_RX14+	
A26	PCIE_TX14-		B26	PCIE_RX14-	
A27	BATLOW#		B27	WDT	
A28	(S)ATA_ACT#		B28	RSVD	
A29	RSVD		B29	RSVD	
A30	RSVD		B30	RSVD	
A31	GND(FIXED)		B31	GND(FIXED)	
A32	RSVD		B32	SPKR	

Connector Rows A and B

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
A33	RSVD		B33	I2C_CK	
A34	BIOS_DIS0#/ESPI_SAFS	BIOS_DIS0#	B34	I2C_DAT	
A35	THRMTRIP#		B35	THRM#	
A36	PCIE_TX13+		B36	PCIE_RX13+	
A37	PCIE_TX13-		B37	PCIE_RX13-	
A38	GND		B38	GND	
A39	PCIE_TX12+		B39	PCIE_RX12+	
A40	PCIE_TX12-		B40	PCIE_RX12-	
A41	GND(FIXED)		B41	GND(FIXED)	
A42	USB2-		B42	USB3-	
A43	USB2+		B43	USB3+	
A44	USB_2_3_OC#		B44	USB_0_1_OC#	
A45	USB0-		B45	USB1-	
A46	USB0+		B46	USB1+	
A47	VCC_RTC		B47	ESPI_EN#	NC
A48	RSVD		B48	USB0_HOST_PRSNT	NC
A49	GBE0_SDP		B49	SYS_RESET#	
A50	LPC_SERIRQ/ESPI_CS1#	LPC_SERIRQ	B50	CB_RESET#	
A51	GND(FIXED)		B51	GND(FIXED)	
A52	PCIE_TX5+		B52	PCIE_RX5+	
A53	PCIE_TX5-		B53	PCIE_RX5-	
A54	GPI0		B54	GPO1	
A55	PCIE_TX4+		B55	PCIE_RX4+	
A56	PCIE_TX4-		B56	PCIE_RX4-	
A57	GND		B57	GPO2	
A58	PCIE_TX3+		B58	PCIE_RX3+	
A59	PCIE_TX3-		B59	PCIE_RX3-	
A60	GND(FIXED)		B60	GND(FIXED)	
A61	PCIE_TX2+		B61	PCIE_RX2+	
A62	PCIE_TX2-		B62	PCIE_RX2-	
A63	GPI1		B63	GPO3	
A64	PCIE_TX1+		B64	PCIE_RX1+	
A65	PCIE_TX1-		B65	PCIE_RX1-	
A66	GND		B66	WAKE0#	
A67	GPI2		B67	WAKE1#	

Connector Rows A and B

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
A68	PCIE_TX0+		B68	PCIE_RX0+	
A69	PCIE_TX0-		B69	PCIE_RX0-	
A70	GND(FIXED)		B70	GND(FIXED)	
A71	PCIE_TX8+		B71	PCIE_RX8+	
A72	PCIE_TX8-		B72	PCIE_RX8-	
A73	GND		B73	GND	
A74	PCIE_TX9+		B74	PCIE_RX9+	
A75	PCIE_TX9-		B75	PCIE_RX9-	
A76	GND		B76	GND	
A77	PCIE_TX10+		B77	PCIE_RX10+	
A78	PCIE_TX10-		B78	PCIE_RX10-	
A79	GND		B79	GND	
A80	GND(FIXED)		B80	GND(FIXED)	
A81	PCIE_TX11+		B81	PCIE_RX11+	
A82	PCIE_TX11-		B82	PCIE_RX11-	
A83	GND		B83	GND	
A84	NCSI_TX_EN		B84	VCC_5V_SBY	
A85	GPI3		B85	VCC_5V_SBY	
A86	RSVD		B86	VCC_5V_SBY	
A87	RSVD		B87	VCC_5V_SBY	
A88	PCIE_CLK_REF+		B88	BIOS_DIS1#	
A89	PCIE_CLK_REF-		B89	NCSI_RX_ER	
A90	GND(FIXED)		B90	GND(FIXED)	
A91	SPI_POWER		B91	NCSI_CLK_IN	
A92	SPI_MISO		B92	NCSI_RXD1	
A93	GPO0		B93	NCSI_RXD0	
A94	SPI_CLK		B94	NCSI_CRS_DV	
A95	SPI_MOSI		B95	NCSI_TXD1	
A96	TPM_PP		B96	NCSI_TXD0	
A97	TYPE10#	NC	B97	SPI_CS#	
A98	SER0_TX		B98	NCSI_ARB_IN	
A99	SER0_RX		B99	NCSI_ARB_OUT	
A100	GND(FIXED)		B100	GND(FIXED)	
A101	SER1_TX/CAN_TX	SER1_TX	B101	FAN_PWMOUT	
A102	SER1_RX/CAN_RX	SER1_RX	B102	FAN_TACHIN	

Connector Rows A and B

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
A103	LID#		B103	SLEEP#	
A104	VCC_12V		B104	VCC_12V	
A105	VCC_12V		B105	VCC_12V	
A106	VCC_12V		B106	VCC_12V	
A107	VCC_12V		B107	VCC_12V	
A108	VCC_12V		B108	VCC_12V	
A109	VCC_12V		B109	VCC_12V	
A110	GND(FIXED)		B110	GND(FIXED)	

Connector Rows C and D

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
C1	GND(FIXED)		D1	GND(FIXED)	
C2	GND		D2	GND	
C3	USB_SSRX0-		D3	USB_SSTX0-	
C4	USB_SSRX0+		D4	USB_SSTX0+	
C5	GND		D5	GND	
C6	USB_SSRX1-		D6	USB_SSTX1-	
C7	USB_SSRX1+		D7	USB_SSTX1+	
C8	GND		D8	GND	
C9	USB_SSRX2-		D9	USB_SSTX2-	
C10	USB_SSRX2+		D10	USB_SSTX2+	
C11	GND(FIXED)		D11	GND(FIXED)	
C12	USB_SSRX3-		D12	USB_SSTX3-	
C13	USB_SSRX3+		D13	USB_SSTX3+	
C14	GND		D14	GND	
C15	10G_PHY_MDC_SCL3	NC	D15	10G_PHY_MDIO_SDA3	NC
C16	10G_PHY_MDC_SCL2	NC	D16	10G_PHY_MDIO_SCL2	NC
C17	10G_SDP2	NC	D17	10G_SDP3	NC
C18	GND		D18	GND	
C19	PCIE_RX6+		D19	PCIE_TX6+	
C20	PCIE_RX6-		D20	PCIE_TX6-	
C21	GND(FIXED)		D21	GND(FIXED)	
C22	PCIE_RX7+		D22	PCIE_TX7+	
C23	PCIE_RX7-		D23	PCIE_TX7-	
C24	10G_INT2	NC	D24	10G_INT3	NC
C25	GND		D25	GND	
C26	10G_KR_RX3+	NC	D26	10G_KR_TX3+	NC
C27	10G_KR_RX3-	NC	D27	10G_KR_TX3-	NC
C28	GND		D28	GND	
C29	10G_KR_RX2+	NC	D29	10G_KR_TX2+	NC
C30	10G_KR_RX2-	NC	D30	10G_KR_TX2-	NC
C31	GND(FIXED)		D31	GND(FIXED)	
C32	10G_SFP_SDA3	NC	D32	10G_SFP_SCL3	NC
C33	10G_SFP_SDA2	NC	D33	10G_SFP_SCL2	NC
C34	10G_PHY_RST_23	NC	D34	10G_PHY_CAP_23	NC
C35	10G_PHY_RST_01		D35	10G_PHY_CAP_01	
C36	10G_LED_SDA		D36	RSVD	

Connector Rows C and D

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
C37	10G_LED_SCL		D37	RSVD	
C38	10G_SFP_SDA1		D38	10G_SFP_SCL1	
C39	10G_SFP_SDA0		D39	10G_SFP_SCL0	
C40	10G_SDP0		D40	10G_SDP1	
C41	GND(FIXED)		D41	GND(FIXED)	
C42	10G_KR_RX1+		D42	10G_KR_TX1+	
C43	10G_KR_RX1-		D43	10G_KR_TX1-	
C44	GND		D44	GND	
C45	10G_PHY_MDC_SCL1		D45	10G_PHY_MDIO_SDA1	
C46	10G_PHY_MDC_SCL0		D46	10G_PHY_MDIO_SDA0	
C47	10G_INT0		D47	10G_INT1	
C48	GND		D48	GND	
C49	10G_KR_RX0+		D49	10G_KR_TX0+	
C50	10G_KR_RX0-		D50	10G_KR_TX0-	
C51	GND(FIXED)		D51	GND(FIXED)	
C52	PCIE_RX16+		D52	PCIE_TX16+	
C53	PCIE_RX16-		D53	PCIE_TX16-	
C54	TYPE0#	GND	D54	RSVD	
C55	PCIE_RX17+		D55	PCIE_TX17+	
C56	PCIE_RX17-		D56	PCIE_TX17-	
C57	TYPE1#	NC	D57	TYPE2#	GND
C58	PCIE_RX18+		D58	PCIE_TX18+	
C59	PCIE_RX18-		D59	PCIE_TX18--	
C60	GND(FIXED)		D60	GND(FIXED)	
C61	PCIE_RX19+		D61	PCIE_TX19+	
C62	PCIE_RX19-		D62	PCIE_TX19-	
C63	RSVD		D63	RSVD	
C64	RSVD		D64	RSVD	
C65	PCIE_RX20+		D65	PCIE_TX20+	
C66	PCIE_RX20-		D66	PCIE_TX20-	
C67	RAPID_SHUTDOWN	NC	D67	GND	
C68	PCIE_RX21+		D68	PCIE_TX21+	
C69	PCIE_RX21-		D69	PCIE_TX21-	
C70	GND(FIXED)		D70	GND(FIXED)	
C71	PCIE_RX22+		D71	PCIE_TX22+	

Connector Rows C and D

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
C72	PCIE_RX22-		D72	PCIE_TX22-	
C73	GND		D73	GND	
C74	PCIE_RX23+		D74	PCIE_TX23+	
C75	PCIE_RX23-		D75	PCIE_TX23-	
C76	GND		D76	GND	
C77	RSVD		D77	RSVD	
C78	PCIE_RX24+		D78	PCIE_TX24+	
C79	PCIE_RX24-		D79	PCIE_TX24-	
C80	GND(FIXED)		D80	GND(FIXED)	
C81	PCIE_RX25+		D81	PCIE_TX25+	
C82	PCIE_RX25-		D82	PCIE_TX25-	
C83	RSVD		D83	RSVD	
C84	GND		D84	GND	
C85	PCIE_RX26+		D85	PCIE_TX26+	
C86	PCIE_RX26-		D86	PCIE_TX26-	
C87	GND		D87	GND	
C88	PCIE_RX27+		D88	PCIE_TX27+	
C89	PCIE_RX27-		D89	PCIE_TX27-	
C90	GND(FIXED)		D90	GND(FIXED)	
C91	PCIE_RX28+		D91	PCIE_TX28+	
C92	PCIE_RX28-		D92	PCIE_TX28-	
C93	GND		D93	GND	
C94	PCIE_RX29+		D94	PCIE_TX29+	
C95	PCIE_RX29-		D95	PCIE_TX29-	
C96	GND		D96	GND	
C97	RSVD		D97	RSVD	
C98	PCIE_RX30+		D98	PCIE_TX30+	
C99	PCIE_RX30-		D99	PCIE_TX30-	
C100	GND(FIXED)		D100	GND(FIXED)	
C101	PCIE_RX31+		D101	PCIE_TX31+	
C102	PCIE_RX31-		D102	PCIE_TX31-	
C103	GND		D103	GND	
C104	VCC_12V		D104	VCC_12V	
C105	VCC_12V		D105	VCC_12V	
C106	VCC_12V		D106	VCC_12V	

Connector Rows C and D

Pin#	Type 7 Description	SOM-5992 Difference	Pin#	Type 7 Description	SOM-5992 Difference
C107	VCC_12V		D107	VCC_12V	
C108	VCC_12V		D108	VCC_12V	
C109	VCC_12V		D109	VCC_12V	
C110	GND(FIXED)		D110	GND(FIXED)	

2.3 General Purpose PCI Express Lanes

The number of available PCI Express lanes varies with the Module Pin-out Type (refer to Section 2.3.2 'PCI Express Link Configuration '). If the Module supports off-Module x16 PCI Express Graphics, then PCI Express Lanes 16-31 ***shall*** be used to implement this.

2.3.1 General Purpose PCIe Signal Definitions

Table 4: General Purpose PCI Express Signal Descriptions

Signal	Pin#	Description	I/O	Note
PCIE_RX0+ PCIE_RX0-	B68 B69	PCIe channel 0. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near COME to PCIE0 x1 device PETp/n0. Slot - Connect to PCIE0 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX0+ PCIE_TX0-	A68 A69	PCIe channel 0. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE0 x1 device PERp/n0. Slot - Connect to PCIE0 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2
PCIE_RX1+ PCIE_RX1-	B64 B65	PCIe channel 1. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE1 x1 device PETp/n0. Slot - Connect to PCIE1 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX1+ PCIE_TX1-	A64 A65	PCIe channel 1. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE1 x1 device PERp/n0. Slot - Connect to PCIE1 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2

Signal	Pin#	Description	I/O	Note
PCIE_RX2+ PCIE_RX2-	B61 B62	PCIe channel 2. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near COME to PCIE2 x1 device PETp/n0. Slot - Connect to PCIE2 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX2+ PCIE_TX2-	A61 A62	PCIe channel 2. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE2 x1 device PERp/n0. Slot - Connect to PCIE2 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2
PCIE_RX3+ PCIE_RX3-	B58 B59	PCIe channel 3. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE3 x1 device PETp/n0. Slot - Connect to PCIE3 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX3+ PCIE_TX3-	A58 A59	PCIe channel 3. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE3 x1 device PERp/n0. Slot - Connect to PCIE3 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2
PCIE_RX4+ PCIE_RX4-	B55 B56	PCIe channel 4. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE4 x1 device PETp/n0. Slot - Connect to PCIE4 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2

Signal	Pin#	Description	I/O	Note
PCIE_TX4+ PCIE_TX4-	A55 A56	PCIe channel 4. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE4 x1 device PERp/n0. Slot - Connect to PCIE4 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2
PCIE_RX5+ PCIE_RX5-	B52 B53	PCIe channel 5. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE5 x1 device PETp/n0. Slot - Connect to PCIE5 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX5+ PCIE_TX5-	A52 A53	PCIe channel 5. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE5 x1 device PERp/n0. Slot - Connect to PCIE5 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2
PCIE_RX6+ PCIE_RX6-	C19 C20	PCIe channel 6. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE5 x1 device PETp/n0. Slot - Connect to PCIE5 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	2
PCIE_TX6+ PCIE_TX6-	D19 D20	PCIe channel 6. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE6 x1 device PERp/n0. Slot - Connect to PCIE6 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	2

Signal	Pin#	Description	I/O	Note
PCIE_RX7+ PCIE_RX7-	C22 C23	PCIe channel 7. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE6 x1 device PETp/n0. Slot - Connect to PCIE6 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	1, 2
PCIE_TX7+ PCIE_TX7-	D22 D23	PCIe channel 7. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE7 x1 device PERp/n0. Slot - Connect to PCIE7 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	1, 2
PCIE_RX8+ PCIE_RX8-	B71 B71	PCIe channel 8. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX8+ PCIE_TX8-	A71 A72	PCIe channel 8. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX9+ PCIE_RX9-	B74 B75	PCIe channel 9. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX9+ PCIE_TX9-	A74 A75	PCIe channel 9. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX10+ PCIE_RX10-	B77 B78	PCIe channel 10. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX10+ PCIE_TX10-	A77 A78	PCIe channel 10. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX11+ PCIE_RX11-	B81 B82	PCIe channel 11. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX11+ PCIE_TX11-	A81 A82	PCIe channel 11. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX12+ PCIE_RX12-	B39 B40	PCIe channel 12. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX12+ PCIE_TX12-	A39 A40	PCIe channel 12. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX13+ PCIE_RX13-	B36 B37	PCIe channel 13. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX13+ PCIE_TX13-	A36 A37	PCIe channel 13. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX14+ PCIE_RX14-	B25 B26	PCIe channel 14. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX14+ PCIE_TX14-	A25 A26	PCIe channel 14. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX15+ PCIE_RX15-	B22 B23	PCIe channel 15. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX15+ PCIE_TX15-	A22 A23	PCIe channel 15. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX16+ PCIE_RX16-	C52 C53	PCIe channel 16. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX16+ PCIE_TX16-	D52 D53	PCIe channel 16. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX17+ PCIE_RX17-	C55 C56	PCIe channel 17. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX17+ PCIE_TX17-	D55 D56	PCIe channel 17. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX18+ PCIE_RX18-	C58 C59	PCIe channel 18. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX18+ PCIE_TX18-	D58 D59	PCIe channel 18. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX19+ PCIE_RX19-	C61 C62	PCIe channel 19. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX19+ PCIE_TX19-	D61 D61	PCIe channel 19. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX20+ PCIE_RX20-	C65 C66	PCIe channel 20. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX20+ PCIE_TX20-	D65 D66	PCIe channel 20. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX21+ PCIE_RX21-	C68 C69	PCIe channel 21. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX21+ PCIE_TX21-	D68 D69	PCIe channel 21. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX22+ PCIE_RX22-	C71 C72	PCIe channel 22. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX22+ PCIE_TX22-	D71 D72	PCIe channel 22. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX23+ PCIE_RX23-	C74 C75	PCIe channel 23. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX23+ PCIE_TX23-	D74 D75	PCIe channel 23. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX24+ PCIE_RX24-	C78 C79	PCIe channel 24. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX24+ PCIE_TX24-	D78 D79	PCIe channel 24. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX25+ PCIE_RX25-	C81 C82	PCIe channel 25. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX25+ PCIE_TX25-	D81 D82	PCIe channel 25. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX26+ PCIE_RX26-	C85 C86	PCIe channel 26. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX26+ PCIE_TX26-	D85 D86	PCIe channel 26. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX27+ PCIE_RX27-	C88 C89	PCIe channel 27. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX27+ PCIE_TX27-	D88 D89	PCIe channel 27. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX28+ PCIE_RX28-	C91 C92	PCIe channel 28. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX28+ PCIE_TX28-	D91 D92	PCIe channel 28. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX29+ PCIE_RX29-	C94 C95	PCIe channel 29. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX29+ PCIE_TX29-	D94 D95	PCIe channel 29. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3

Signal	Pin#	Description	I/O	Note
PCIE_RX30+ PCIE_RX30-	C98 C99	PCIe channel 30. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX30+ PCIE_TX30-	D98 D99	PCIe channel 30. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_RX31+ PCIE_RX31-	C101 C102	PCIe channel 31. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near to PCIE device PETp/nX. N/C if not used.	I PCIE	3
PCIE_TX31+ PCIE_TX31-	D101 D102	PCIe channel 31. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE device PERp/nX. N/C if not used.	O PCIE	3
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE	

Notes:

1. SOM-5992 Default : I210.
2. Only support PCIe Gen2.
3. The AC Coupling cap 0.1uF is used for Gen2 and 0.22uF is used for Gen3.

2.3.2 PCI Express Lane Configurations – SOM-5992 Type 7 Limitations

Table 5: SOM-5992 PCI Express Lane Configurations

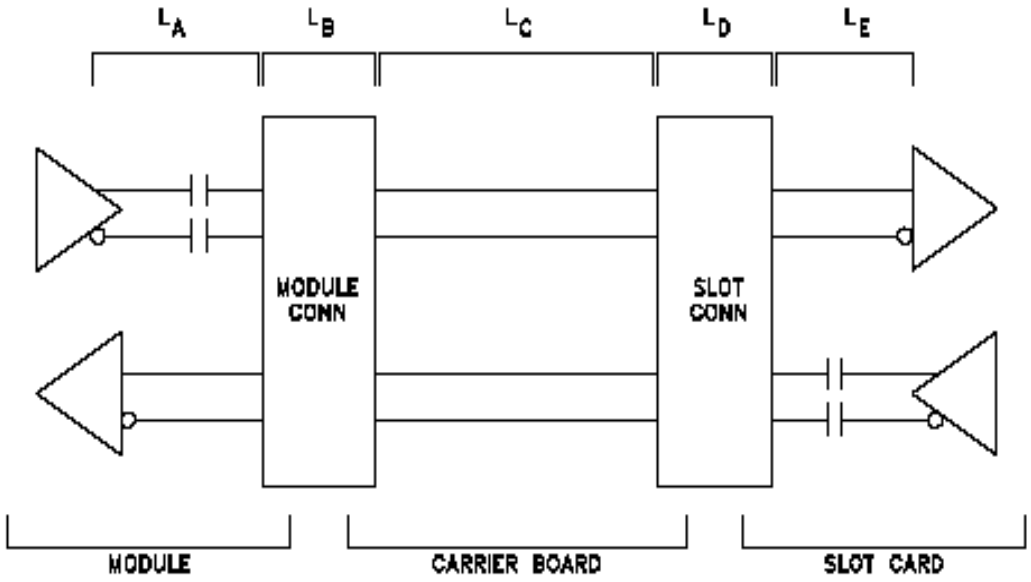
B2B Pin				Signal	Link Width	
A68	PCIE_TX0+	B68	PCIE_RX0+	PCIE1X0	X1	
A69	PCIE_TX0-	B69	PCIE_RX0-			
A64	PCIE_TX1+	B64	PCIE_RX1+	PCIE1X1	X1	
A65	PCIE_TX1-	B65	PCIE_RX1-			
A61	PCIE_TX2+	B61	PCIE_RX2+	PCIE1X2	X1	
A62	PCIE_TX2-	B62	PCIE_RX2-			
A58	PCIE_TX3+	B58	PCIE_RX3+	PCIE1X3	X1	
A59	PCIE_TX3-	B59	PCIE_RX3-			
A55	PCIE_TX4+	B55	PCIE_RX4+	PCIE1X4	X1	
A56	PCIE_TX4-	B56	PCIE_RX4-			
A52	PCIE_TX5+	B52	PCIE_RX5+	PCIE1X5	X1	
A53	PCIE_TX5-	B53	PCIE_RX5-			
D19	PCIE_TX6+	C19	PCIE_RX6+	PCIE1X6	X1	
D20	PCIE_TX6-	C20	PCIE_RX6-			
D22	PCIE_TX7+	C22	PCIE_RX7+	PCIE1X7	Default : I210 Option : X1	
D23	PCIE_TX7-	C23	PCIE_RX7-			
A71	PCIE_TX8+	B71	PCIE_RX8+	PCIE8X0	X4	X8
A72	PCIE_TX8-	B72	PCIE_RX8-			
A74	PCIE_TX9+	B74	PCIE_RX9+	PCIE8X1		
A75	PCIE_TX9-	B75	PCIE_RX9-			
A77	PCIE_TX10+	B77	PCIE_RX10+	PCIE8X2		
A78	PCIE_TX10-	B78	PCIE_RX10-			
A81	PCIE_TX11+	B81	PCIE_RX11+	PCIE8X3		
A82	PCIE_TX11-	B82	PCIE_RX11-			
A39	PCIE_TX12+	B39	PCIE_RX12+	PCIE8X4	X4	
A40	PCIE_TX12-	B40	PCIE_RX12-			
A36	PCIE_TX13+	B36	PCIE_RX13+	PCIE8X5		
A37	PCIE_TX13-	B37	PCIE_RX13-			
A25	PCIE_TX14+	B25	PCIE_RX14+	PCIE8X6		
A26	PCIE_TX14-	B26	PCIE_RX14-			
A22	PCIE_TX15+	B22	PCIE_RX15+	PCIE8X7		
A23	PCIE_TX15-	B23	PCIE_RX15-			

D52	PCIE_TX16+	C52	PCIE_RX16+	PCIE16X0	X4	X8	X16
D53	PCIE_TX16-	C53	PCIE_RX16-				
D55	PCIE_TX17+	C55	PCIE_RX17+	PCIE16X1			
D56	PCIE_TX17-	C56	PCIE_RX17-				
D58	PCIE_TX18+	C58	PCIE_RX18+	PCIE16X2			
D59	PCIE_TX18-	C59	PCIE_RX18-				
D61	PCIE_TX19+	C61	PCIE_RX19+	PCIE16X3			
D62	PCIE_TX19-	C62	PCIE_RX19-				
D65	PCIE_TX20+	C65	PCIE_RX20+	PCIE16X4	X4		
D66	PCIE_TX20-	C66	PCIE_RX20-				
D68	PCIE_TX21+	C68	PCIE_RX21+	PCIE16X5			
D69	PCIE_TX21-	C69	PCIE_RX21-				
D71	PCIE_TX22+	C71	PCIE_RX22+	PCIE16X6			
D72	PCIE_TX22-	C72	PCIE_RX22-				
D74	PCIE_TX23+	C74	PCIE_RX23+	PCIE16X7			
D75	PCIE_TX23-	C75	PCIE_RX23-				
D78	PCIE_TX24+	C78	PCIE_RX24+	PCIE16X8	X4	X8	
D79	PCIE_TX24-	C79	PCIE_RX24-				
D81	PCIE_TX25+	C81	PCIE_RX25+	PCIE16X9			
D82	PCIE_TX25-	C82	PCIE_RX25-				
D85	PCIE_TX26+	C85	PCIE_RX26+	PCIE16X10			
D86	PCIE_TX26-	C86	PCIE_RX26-				
D88	PCIE_TX27+	C88	PCIE_RX27+	PCIE16X11			
D89	PCIE_TX27-	C89	PCIE_RX27-				
D91	PCIE_TX28+	C91	PCIE_RX28+	PCIE16X12	X4		
D92	PCIE_TX28-	C92	PCIE_RX28-				
D94	PCIE_TX29+	C94	PCIE_RX29+	PCIE16X13			
D95	PCIE_TX29-	C95	PCIE_RX29-				
D98	PCIE_TX30+	C98	PCIE_RX30+	PCIE16X14			
D99	PCIE_TX30-	C99	PCIE_RX30-				
D101	PCIE_TX31+	C101	PCIE_RX31+	PCIE16X15			
D102	PCIE_TX31-	C102	PCIE_RX31-				

2.3.3 PCI Express General Routing Guidelines

2.3.3.1 PCI Express Insertion Loss Budget with Slot Card

Figure 3: PCI Express Insertion Loss Budget with Slot Card



The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget shall be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget shall be 3.46 dB. COM Express connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are the same in this case. The Carrier Board insertion loss budget shall be 4.40 dB. COM Express connector and slot card connector losses are accounted for separately.

The slot card transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the slot card's transmit path. The slot card's transmit path insertion loss budget is 3.84 dB (2.65 dB + 1.19 dB) per the PCI Express Card Electromechanical Specification Revision 1.1. The slot card's receive path insertion loss budget is 2.65 dB per the same specification. Slot card connector loss is accounted for separately.

Table 6: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board Slot Card

Segment	**Loss (dB) max. Length [mm/inches]**	Notes
L_A	130/5.15	Allowance for 5.15 inches of module trace 3.45 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express™ connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	228/9.0	Allowance for 9 inches of Carrier Board trace 4.40 db loss @ 0.28 dB / GHz / inch and a 1.25 dB crosstalk allowance.
L_D		1.25 dB loss. PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss.
L_E		2.65 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1(without coupling caps; L_{AR}). Implied crosstalk allowance is 1.25 dB.
Total		13.20 dB loss.

PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board Slot Card

For “device up” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 4.45 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics.

Other dielectrics with lower losses could be considered, but were not simulated

.

It can be noted that a use case exists that might result in reduced PCI Express bandwidth. This use case is tied to Carrier boards with a PCI Express slot (device up). PCI Express Gen 1 and Gen 2 signaling rates use the same PCI Express connector – there is no mechanical keying mechanism to identify the capabilities of the PCI Express slot or the PCI Express board plugged into the slot. This can lead to the situation where the Module and PCI Express board attempt a PCI Express Gen2 signaling rate connection over a Carrier that does not meet the routing guidelines for Gen 2 signaling rates. In a worst case scenario the devices might connect at Gen2 signaling rate with a high number of errors impacting the actual data throughput. It should be noted that there is a Carrier EEPROM which would allow the Module to determine the Carrier Board capabilities but this is not a requirement in COM.0.

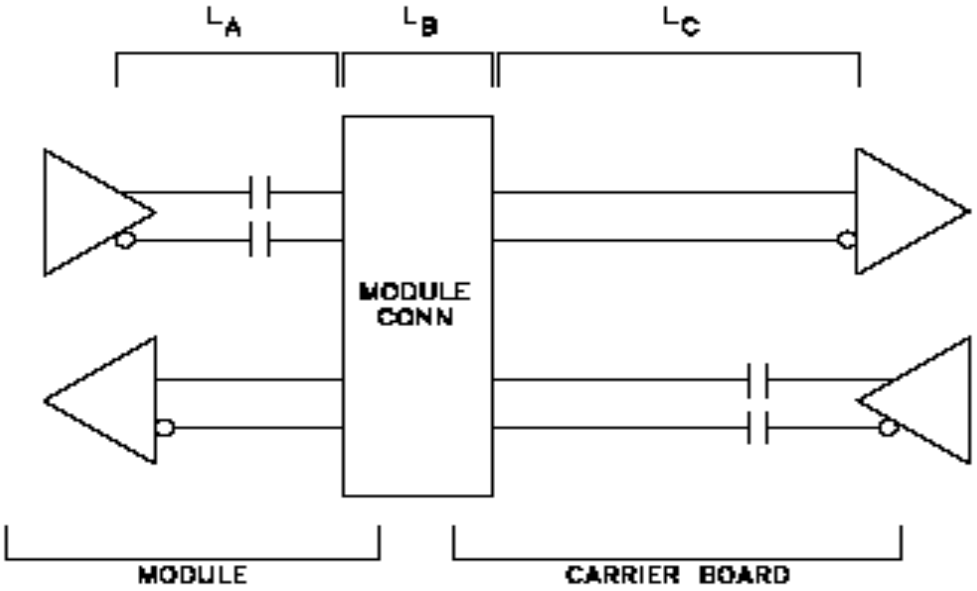
Table 7: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board Slot Card

Segment	**max. Length [mm/inches]**	Notes
L_A	127/5.0	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	113/4.45	Allowance for Carrier Board.
L_D		PCI Express Card slot connector simulated at 2.5 GHz.
L_E	80/3.15	Slot Card trace length from PCI Express Card Electromagnetical Spec., Rev. 1.1
Total	320/12.6	PCIe GEN2 Data clocked architecture

2.3.3.2 PCI Express Insertion Loss Budget with Carrier Board PCIE Device

The insertion losses previously allowed for the slot card and slot card connector are reallocated for use on the Carrier Board, allowing longer Carrier Board trace lengths and more Carrier Board design flexibility. The Module and COM Express connector loss budgets remain the same.

Figure 4: PCI Express Insertion Loss Budget with Carrier Board PCIe Device



The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget shall be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget shall be 3.46 dB. COM ExpressTM connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Carrier Board transmit path. The Carrier Board transmit path insertion loss budget shall be 9.49 dB (8.30 dB + 1.19 dB). The Carrier Board receive path insertion loss shall be 8.30 dB. COM Express connector loss is accounted for separately.

Table 8: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIe Device

Segment	**Loss (dB)** **max. Length** **[mm/inches]**	Notes
L_A	131/5.15	Allowance for 3.46 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (LST– LSR). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	402/15.85	Allowance for 8.30 dB loss @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance..
Total	13.2	13.2dB loss

PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board PCIE Device

For “device down” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 8.0 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

Table 9: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board PCIe Device

Segment	**max. Length** **[mm/inches]**	Notes
L_A	127/5	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	203/8	Allowance for Carrier Board trace.
Total	330/13.0	PCIe GEN2 Data clocked architecture

2.3.4 PCI Express Trace Length Guidelines

Figure 5: Topology for PCI Express Slot Card.

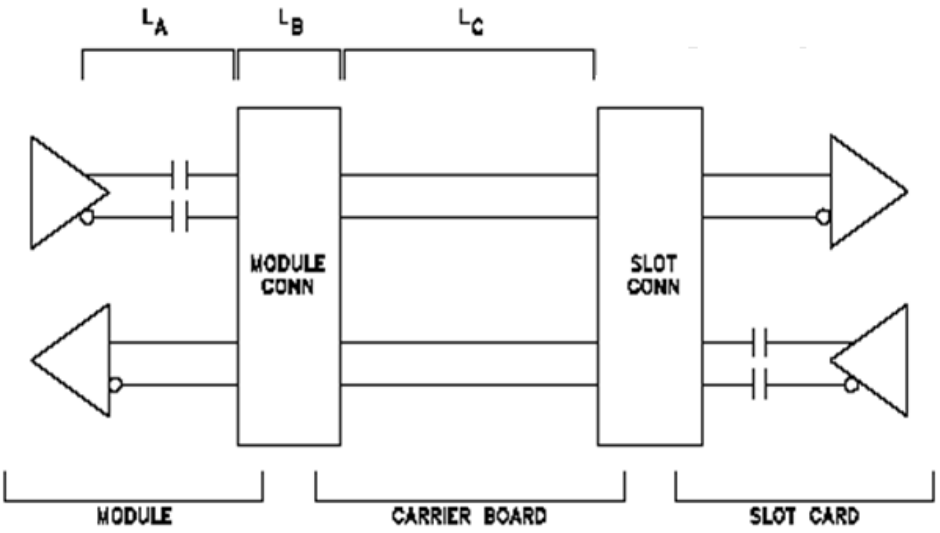


Figure 6: Topology for PCI Express Device Down.

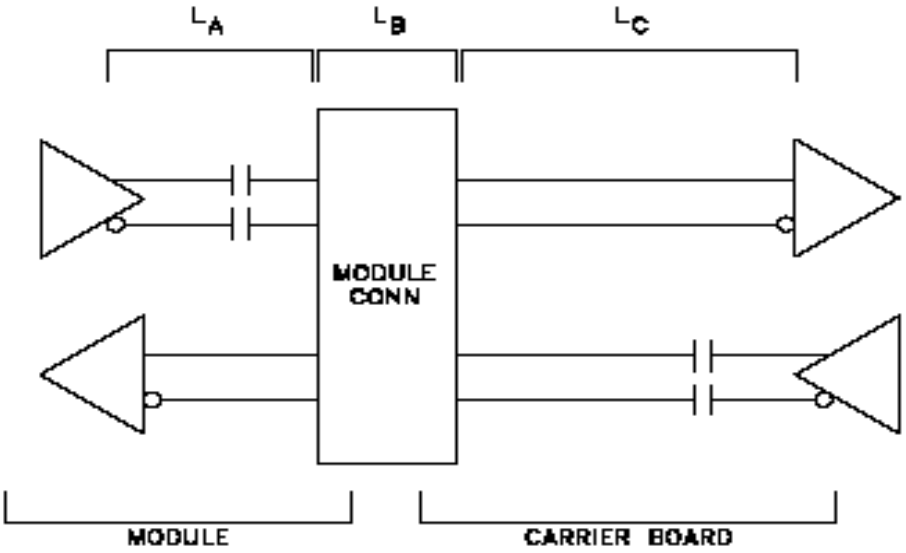


Table 10: PCI Express* Slot Card / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	PCI Express* expansion	
Differential Impedance Target	85Ω±10%	
Single End	55Ω±10%	
Isolation to equivalent pairs	11H (MS) and 3H(DS)	1,2
Isolation to other signal groups	11H (MS) and 5H (DS)	1
Tx/Rx Spacing	11H(MS) and 5H (DS)	1
LA + LB	Please see the SOM-5992 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 14” Device Down:4~ 16”	
Length matching	Differential pairs (intra-pair): Max. 2 mils REFCLK+ and REFCLK- (intra-pair):Max. 5mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias per TX Max. 4 vias per RX (to device) Max. 2 vias per RX (to slot)	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF ±10%, 16V, shape 0402.	3

Notes:

1. H is height above reference plane.
2. Equivalent pairs are TX to TX or RX to RX(Noninterleaved)
3. AC caps are recommended to be placed close to PCIe device side (avoid placing AC cpas on mid-bus).

2.4 NC-SI

2.4.1 NC-SI Signal Definitions

The NC-SI ('Network Controller Sideband Interface') is an electrical interface and protocol defined by the Distributed Management Task Force (DMTF), which enables the connection of a BMC (Baseboard Management Controller) to enable out-of-band remote manageability.

If implemented, the NC-SI ***shall*** be assigned to the **GBE0** interface. NC-SI architecture also enables multiple endpoints to be connected to the same management controller.

In this configuration, the bus arbitration can also be implemented by hardware using a token ring configuration. The NCSI_ARB_IN pin of one controller must be connected to the NCSI_ARB_OUT of another controller to form a ring configuration. A maximum of four network controllers can be connected in this manner and all controllers sharing the same NC-SI interface pins must support this feature in order to use hardware-based arbitration. NCSI_ARB_IN and NCSI_ARB_OUT are to be left unconnected on the Carrier if there is no Carrier network controller.

Table 11: NC-SI Signal Description

Signal	Pin#	Description	I/O	Notes
NCSI_CLK_IN	B91	NC-SI Clock reference for receive, transmit, and control interface.	I COM 3.3V Suspend / 3.3V	
NCSI_RXD0	B93	NC-SI Receive Data (from NC to BMC).	O COM 3.3V Suspend / 3.3V	
NCSI_RXD1	B92	NC-SI Receive Data (from NC to BMC).	O COM 3.3V Suspend / 3.3V	
NCSI_TXD0	B96	NC-SI Transmit Data (from BMC to NC).	I COM 3.3V Suspend / 3.3V	
NCSI_TXD1	B95	NC-SI Transmit Data (from BMC to NC).	I COM 3.3V Suspend / 3.3V	
NCSI_CRS_DV	B94	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O COM 3.3V Suspend / 3.3V	
NCSI_TX_EN	A84	NC-SI Transmit enable.	I COM 3.3V Suspend / 3.3V	
NCSI_RX_ER	B89	NC-SI Receive error.	O COM 3.3V Suspend / 3.3V	
NCSI_ARB_IN	B98	NC-SI hardware arbitration input. N/C if not used.	I COM 3.3V Suspend / 3.3V	
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output. N/C if not used.	O COM 3.3V Suspend / 3.3V	

Notes:

2.4.2 NC-SI General Routing Guidelines

NA

2.4.3 NC-SI Trace Length Guidelines

Figure 7: Topology for NC-SI.

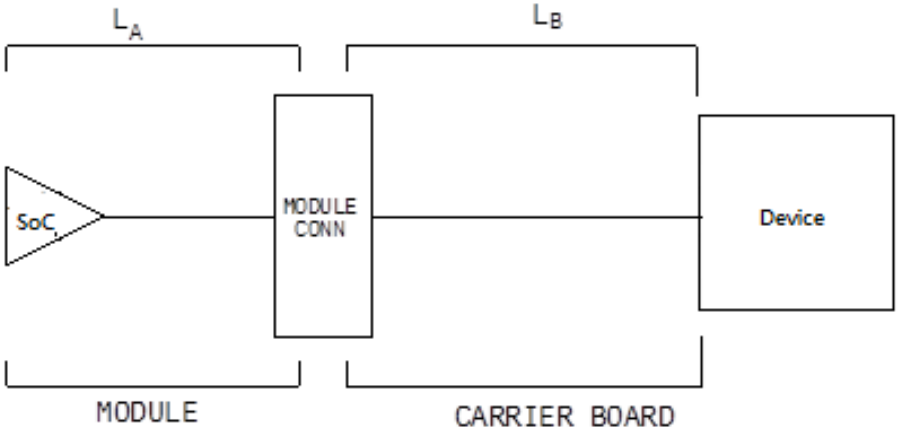


Table 12: NC-SI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	NC-SI	
Single End	50Ω ±10%	
Nominal Trace Space within LPC Signal Group	3H	
Spacing to Other Signal Group	3H	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	8.5” Single source	
Length matching between single ended signals	NA	
Length matching between clock signals	NA	
Reference Plane	GND referencing preferred.	
Via Usage	Try to minimize number of vias	

Notes:

1.H is height above reference plane.

2.5 10GB Ethernet

10GBASE-KR support was added to COM Express with revision 3.0 of the specification.
Type 7 supports up to four 10GBASE-KR interfaces. The 10G MAC is located on the Module and the PHY is located on the Carrier. 10GBASE-KR uses a single transmit and a single receive ac coupled differential pair for data and a sideband bus for the PHY control and configuration. COM Express supports both MDIO and I2C control interfaces for the PHY.

The PHY control interfaces are grouped into pairs. 10G Ports 0 and 1 share a common PHY control interface and 10G ports 2 and 3 share a common PHY control interface. The PHY interface selection is made using the 10G_PHY_CAP_01 and 10G_PHY_CAP_23 pins. The Carrier design can select the PHY that is appropriate for the design. The Module designer ***should*** design the module in such a way that it can provide the PHY interface that is selected regardless of the capabilities of the silicon used on the Module. Appropriate level shifters ***shall*** be used.

A two wire I2C bus (designated 10G_LED_SDA and 10G_LED_SCL) is defined to serialize the outbound (Module to Carrier) MAC LED and PHY strapping signals, conserving COM Express pins. The Carrier ***should*** use a PCA9539 or compatible I2C I/O expander. The Carrier PCA9539 ***shall*** be mapped to I2C address 1110 100x (x=R/W bit). Table 14 below defines the port pin mapping for the I/O expander.

There are two pairs of PHY strapping signals defined. The first pair is designated as 10G_PHY_CAP_01 and 10G_PHY_CAP_23. These are actual COM Express pins. They are inputs to the COM Express Module. The Carrier ***may*** either tie these lines to GND or leave them NC on the Carrier. If 10G_PHY_CAP_01 is tied low on the Carrier, this indicates to the Module that the PHY on the Carrier for 10G interfaces 0 and 1 can be configured by either I2C or by MDIO. If the Carrier leaves the line NC, then this indicates to the Module that the Carrier PHY can only be configured by MDIO. Similarly for strap signal 10G_PHY_CAP_23 and 10G interfaces 2 and 3.

The second pair of PHY strapping signals are outputs from the Module, serialized onto the 10G_LED_Sxx I2C bus. They are desterilized on the Carrier I/O expander and ***may*** used to set Carrier PHY strapping pins to set the desired Carrier PHY configuration mode, if the PHY is capable of multiple configuration modes.

This arrangement with a pair of input straps (telling the Module what configuration modes are possible on the Carrier PHY) and a pair of serialized output straps (telling the Carrier PHY what configuration mode to use) allow Module designs that can use a variety of PHYs. In particular, Intel Broadwell DE Modules that can be used with either Intel "Coppervale" PHYs or with Inphy / Cortina PHYs can be realized. Block diagram examples may be found in 2.5.2 ‘Example 10 GB Ethernet Designs’ of this document.

2.5.1 10GB LAN Signal Definitions

Table 13: 10GB LAN Signal Description

Signal	Pin#	Description	I/O	Notes
10G_KR_TX0+ 10G_KR_TX0-	D49 D50	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR	
10G_KR_RX0+ 10G_KR_RX0-	C49 C50	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR	
10G_KR_TX1+ 10G_KR_TX1-	D42 D43	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR	
10G_KR_RX1+ 10G_KR_RX1-	C42 C43	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR	
10G_KR_TX2+ 10G_KR_TX2-	D29 D30	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR	1
10G_KR_RX2+ 10G_KR_RX2-	C29 C30	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR	1
10G_KR_TX3+ 10G_KR_TX3-	D26 D27	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR	1
10G_KR_RX3+ 10G_KR_RX3-	C26 C27	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR	1

Signal	Pin#	Description	I/O	Notes
10G_PHY_MDIO_SDA0	D46	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_PHY_MDC_SCL0	C46	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_PHY_MDIO_SDA1	D45	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	

Signal	Pin#	Description	I/O	Notes
10G_PHY_MDC_SCL1	C45	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_PHY_MDIO_SDA2	D16	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	1
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_PHY_MDC_SCL2	C16	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	1
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	1

Signal	Pin#	Description	I/O	Notes
10G_PHY_MDIO_SDA3	D15	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	1
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_PHY_MDC_SCL3	C15	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V	1
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_PHY_CAP_01	D35	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface (see Table 13) Carrier board:	I CMOS 3.3V Suspend / 3.3V	

Signal	Pin#	Description	I/O	Notes
10G_PHY_CAP_23	D34	PHY mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface (see Table 13) Carrier board:	I CMOS 3.3V Suspend / 3.3V	1
10G_SFP_SDA0	C39	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_SFP_SCL0	D39	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_SFP_SDA1	C38	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_SFP_SCL1	D38	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	

Signal	Pin#	Description	I/O	Notes
10G_SFP_SDA2	C33	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_SFP_SCL2	D33	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_SFP_SDA3	C32	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_SFP_SCL3	D32	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	1
10G_LED_SCL	C37	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V	
10G_PHY_RST_01	C35	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used). Carrier board:	O CMOS 3.3V Suspend / 3.3V	
10G_PHY_RST_23	C34	Output signal that resets an Optical PHY on port 2 and port 3 (with Copper PHY this signal is not used). Carrier board:	O CMOS 3.3V Suspend / 3.3V	1

Signal	Pin#	Description	I/O	Notes
10G_INT0	C47	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V	
10G_INT1	D47	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V	
10G_INT2	C24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V	1
10G_INT3	D24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V	1
10G_SDP00	C40	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V	
10G_SDP1	D40	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V	
10G_SDP2	C17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V	1
10G_SDP3	D17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V	1
10G_LED_SDA	C36	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.Refer to the details in table 14 'I2C Data Mapping to Carrier Board based PCA9539 I/O expander'	I/O OD CMOS 3.3V Suspend / 3.3V	

Note:

1. SOM-5992 is NC.

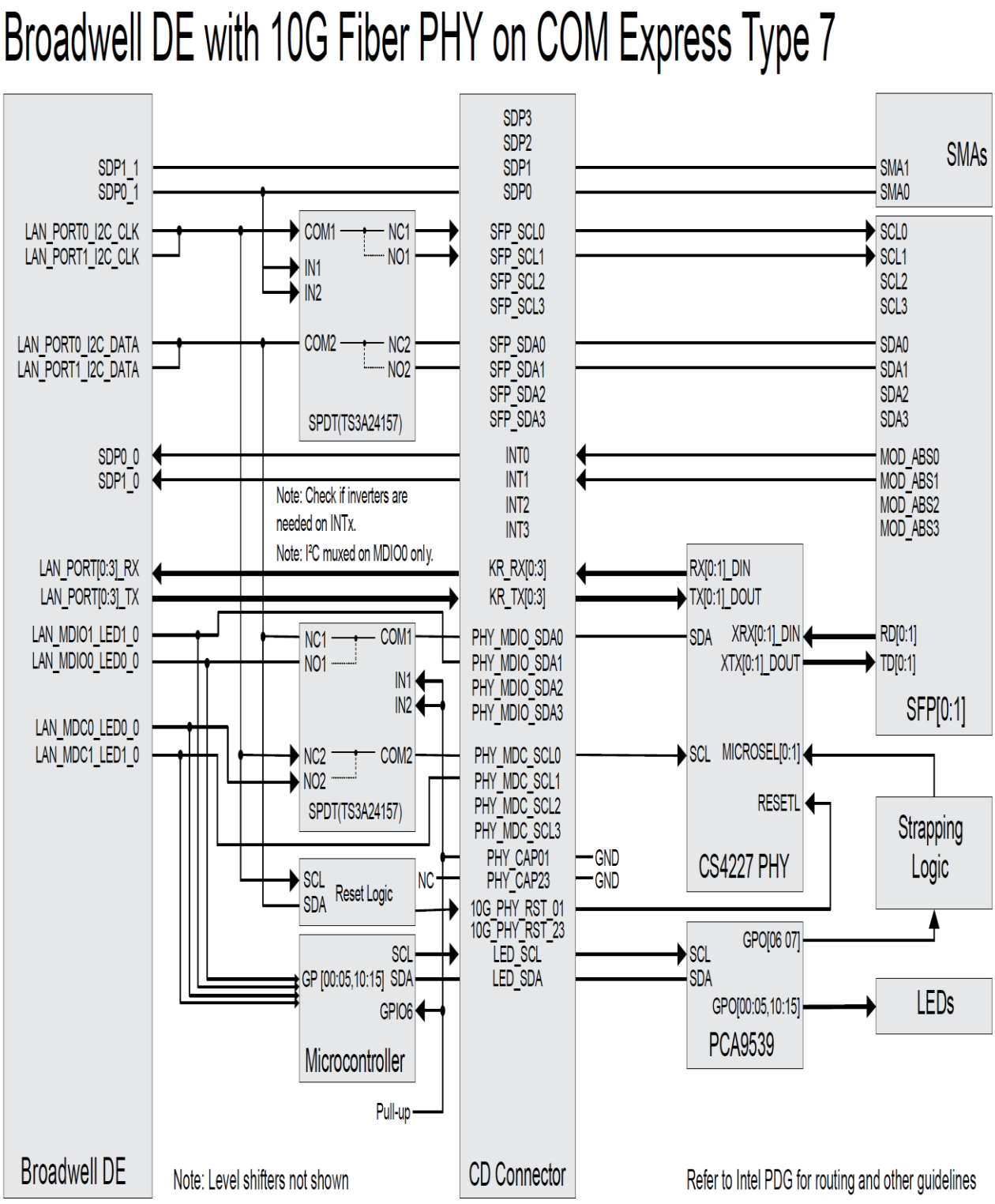
Table 14: I2C Data Mapping to Carrier Board based PCA9539 I/O expander

Port Pin	Signal Name	Signal Function
P0_0	10G_KR_LED0_0#	PHY 0, LED 0 - STATUS/ACT
P0_1	10G_KR_LED0_1#	PHY 0, LED 1 - LINK SPEED MAX
P0_2	10G_KR_LED0_2#	PHY 0, LED 2 - LINK SPEED
P0_3	10G_KR_LED1_0#	PHY 1, LED 0 - STATUS/ACTIVITY
P0_4	10G_KR_LED1_1#	PHY 1, LED 1 - LINK SPEED MAX
P0_5	10G_KR_LED1_2#	PHY 1, LED 2 - LINK SPEED
P0_6	0G_KR_STRAP01	PHY 0-1, 0 = PHY to use I2C, 1 = PHY to use MDIO
P0_7	10G_KR_STRAP23	PHY 2-3, 0 = PHY to use I2C, 1 = PHY to use MDIO
P1_0	10G_KR_LED2_0#	PHY 2, LED 0 - STATUS/ACT
P1_1	10G_KR_LED2_1#	PHY 2, LED 1 - LINK SPEED MAX
P1_2	10G_KR_LED2_2#	PHY 2, LED 2 - LINK SPEED
P1_3	10G_KR_LED3_0#	PHY 3, LED 0 - STATUS/ACT
P1_4	10G_KR_LED3_1#	PHY 3, LED 1 - LINK SPEED MAX
P1_5	10G_KR_LED3_2#	PHY 3, LED 2 - LINK SPEED
P1_6	RSVD	TBD
P1_7	RSVD	TBD

2.5.2 Example 10 GB Ethernet Designs

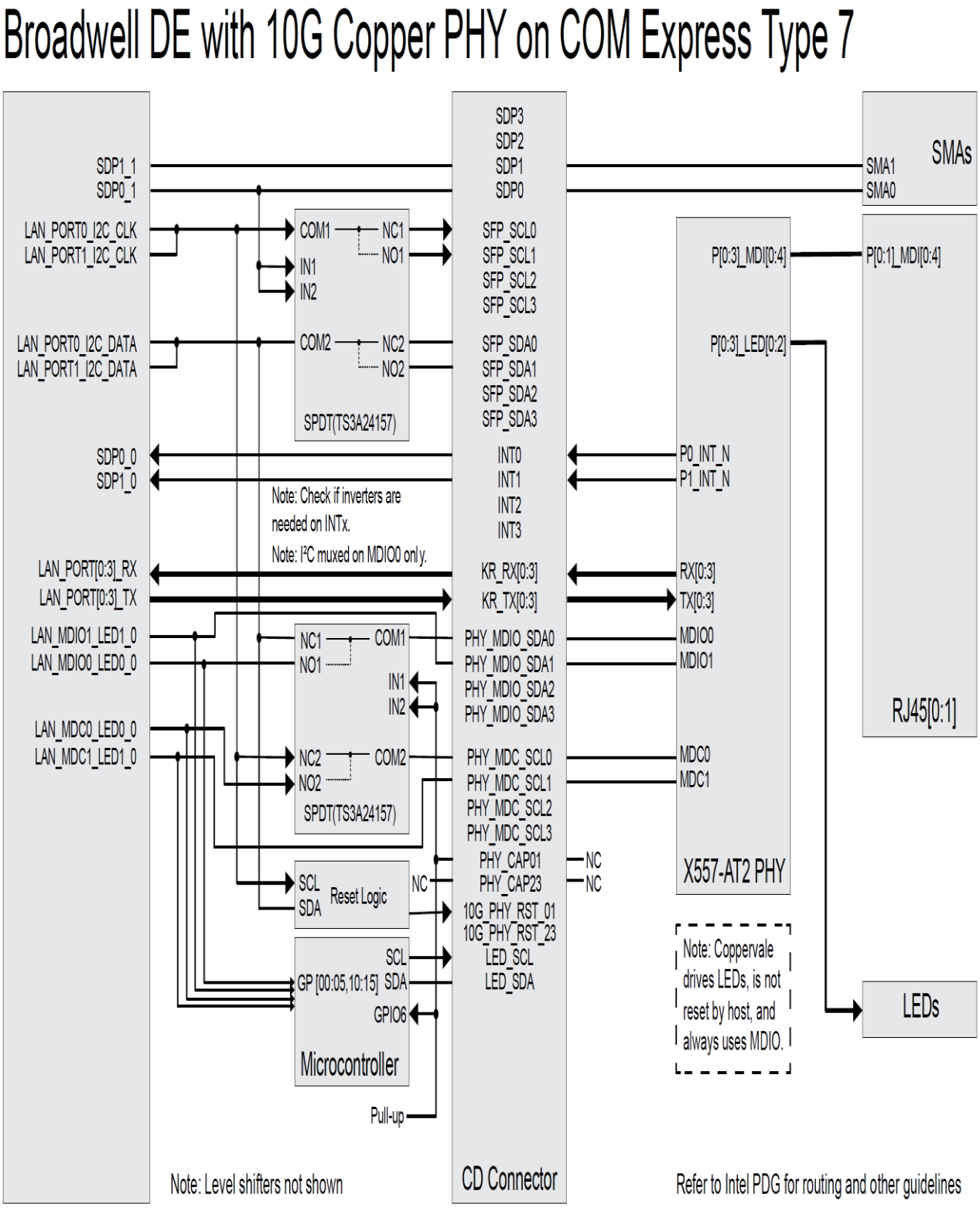
2.5.2.1 2016 Silicon 10GbE Fiber Implementation

Figure 8: 10G Ethernet Design for Fiber PHY with Broadwell DE



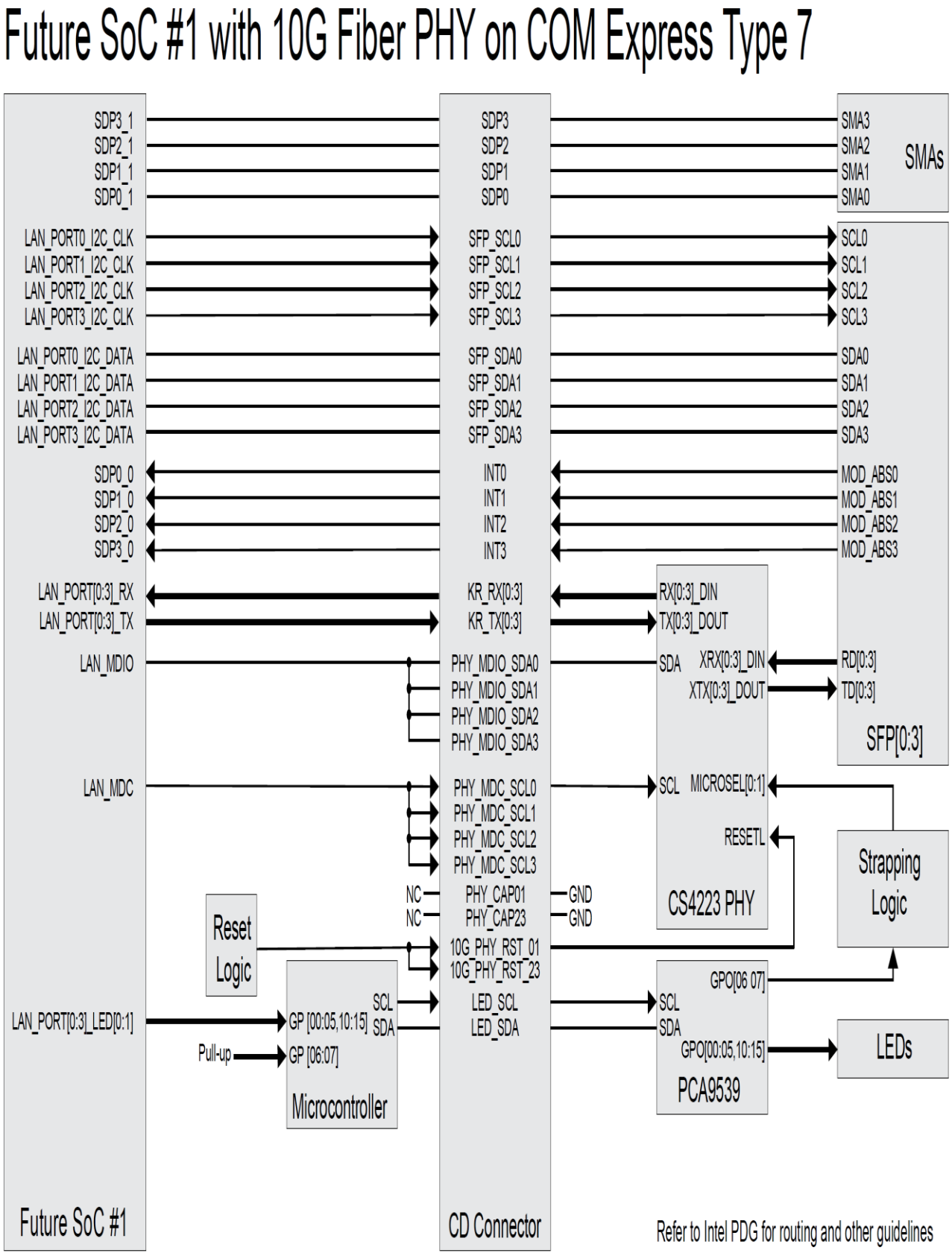
2.5.2.2 2016 Silicon 10GbE Copper Implementation

Figure 9: 10G Ethernet Design for Copper PHY with Broadwell DE



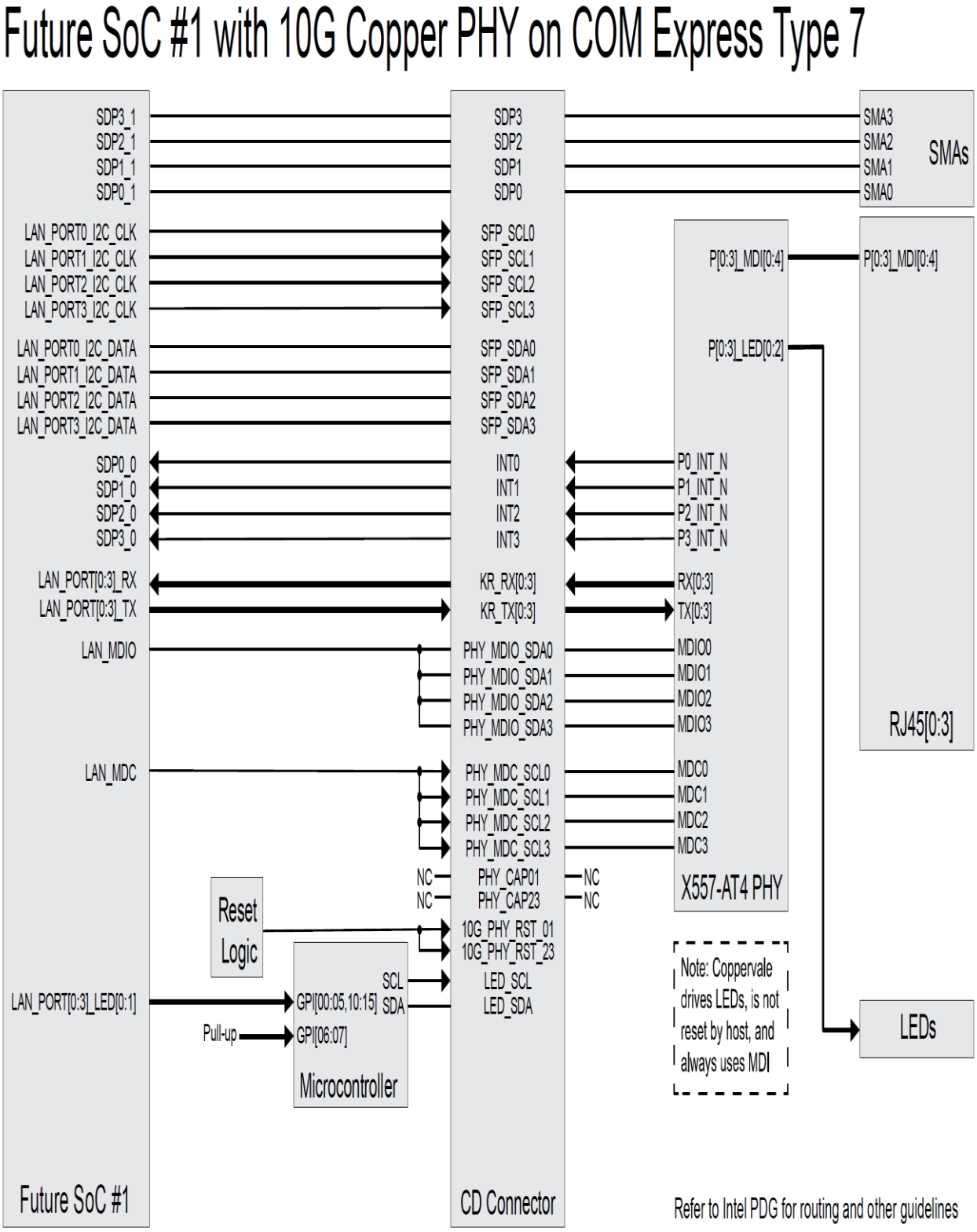
2.5.2.3 Future Silicon 10GbE Fiber Implementation

Figure 10: 10G Ethernet Design for Fiber PHY with Future SoC



2.5.2.4 Future Silicon 10GbE Copper Implementation

Figure 11: 10G Ethernet Design for Copper PHY with Future SoC

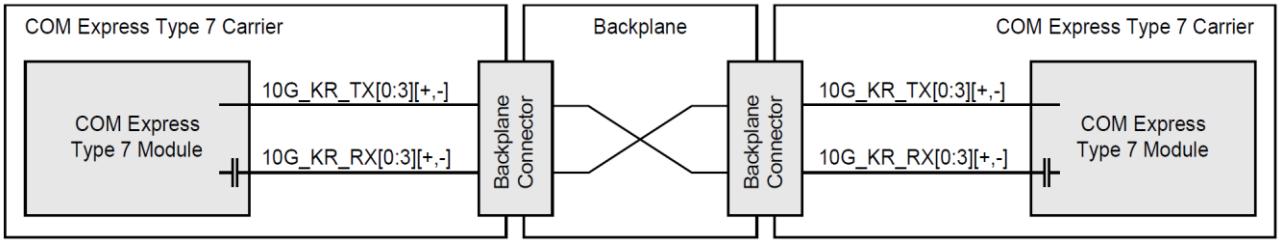


2.5.3 AC Coupling of 10G_KR_TX Signals

Situation A: Backplaned system (eg VPXR, CPCI, ..)

Coupling is at receiver, in this case on both modules at receive pair. No coupling on carrier.

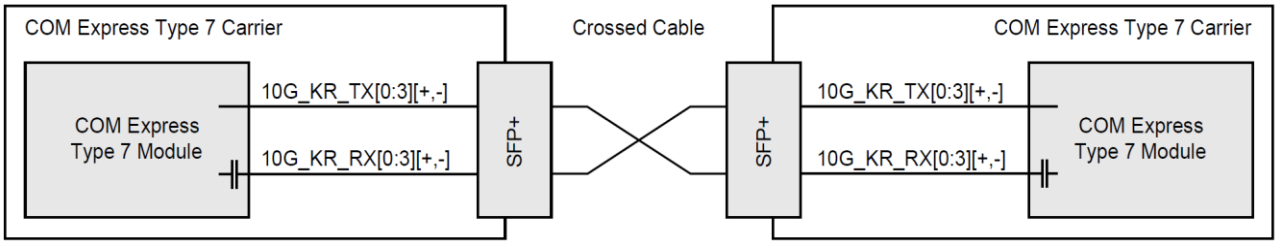
Figure 12: 10G Ethernet AC coupling – backplane system



Situation B: Direct attached module-to-module connection.

Coupling is at receiver, in this case on both modules at receive pair. No coupling on carrier.

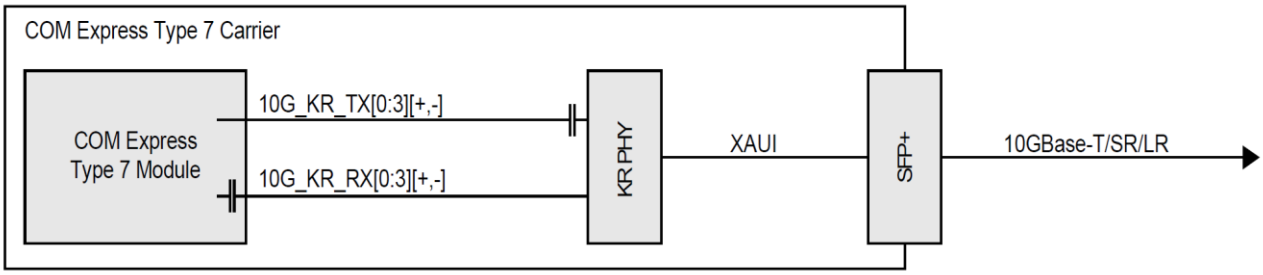
Figure 13: 10G Ethernet AC coupling – direct cable



Situation C: PHY on Carrier

Only in this situation the coupling is on the Carrier (at PHY). But this situation is not the only primary function for KR interface (backplane metallic connection).

Figure 14: 10G Ethernet AC coupling – PHY on Carrier



2.5.4 10GB LAN Routing Guidelines

10Gb Ethernet Insertion Loss Performance

The 10Gb Ethernet interface to the COM Express connector is the KR interface as specified in the IEEE 802.3-KR Clause 72 and Annex 69B specification. This is the MAC to PHY interface as opposed to the PHY to connector (magnetic) interface of the 1Gb Ethernet connections.

Typically, the MAC KR interface is connected directly to the PHY. In the case of COM Express, the KR interface is connected through the COM Express connector to the PHY. The insertion loss performance must be maintained within the normative channel specification as stated in IEEE 802.3 Annex 69B. Simulations have shown that the trace length allocations in Table15 meet the required channel specifications. Proper high speed design techniques must be used. Consult the silicon design guide for trace clearance and other design rules. High speed guidance for the routing of 10GHz differential pairs is outside the scope of this document. All differential pairs are routed at 100 Ohms +/-10% differential impedance Match signals within a pair +/- 5 mils

Figure 15: 10GBASE-KR Trace Length Budget

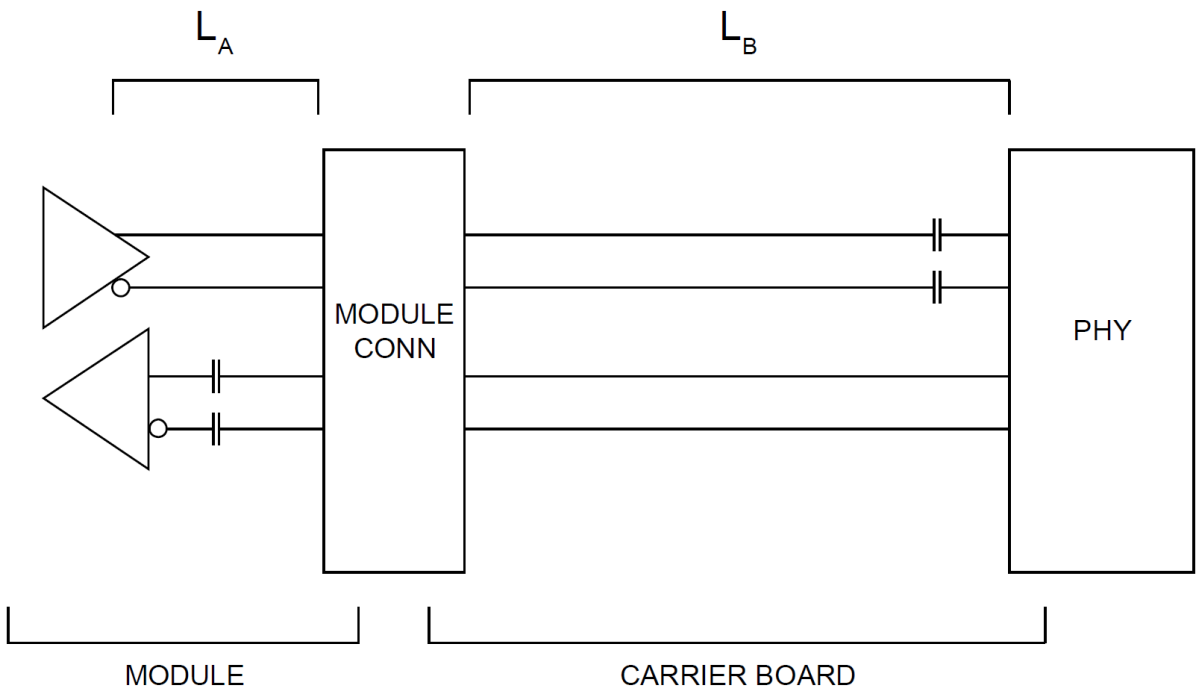


Table 15: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Length (mils)	Notes
L_A	2500	Up to 2.5 inches of Module trace (within Normal FR4)
L_B	5000	Up to 5 inches of Carrier Board trace (within Normal FR4)
Total	7500	

2.5.4.1 10GB LAN KR Guidelines

Table 16: 10GB LAN KR Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	10GB LAN KR	
Differential Impedance Target	100Ω±10%	
Single End	50Ω±10%	
Isolation to equivalent pairs	12H (MS) and 5H(DS)	1,2
Isolation to other signal groups	15H (MS) and 7H (DS)	1
Tx/Rx Spacing	15H(MS) and 7H (DS)	1
LA + LB	SOM-5992 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 28” Device Down: 28”	
Length matching	Differential pairs (intra-pair): Max. ±5mls	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias per TX trace, Max. 3 vias per RX trace	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF ±10%, 16V, shape 0402.	3

Notes:

1.H is height above reference plane.

2.Equivalent pairs are TX to TX or RX to RX(Noninterleaved)

3.AC caps are recommended to be placed close to KR device side (avoid placing AC cpas on mid-bus).

2.5.4.2 10GB LAN Sideban Guidelines

Table 17: 10GB LAN Sideban Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SDP/ MDIO& MDC/LED	
Single End	50Ω ±10%	
Nominal Trace Space within CRT DAC Signal Group	Min. --10mils	
Spacing to Other Signal Group	Min. --10mils	
LA	Please reference SOM-5992 Layout check list	
LB	Carrier Board Length	
Max length of LA+LB	8”	
Length matching	1. Match the trace lengths within MDIO & MDC to ±250 mils.	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

2.6 Gb Ethernet

One Gigabit Ethernet port is defined, designated GBE0. The ports ***may*** operate in 10, 100, or 1000 Mbit/sec modes. Magnetics are assumed to be on the Carrier Board. All COM Express Modules ***shall*** implement at least one Ethernet port on the GBE0 pin slot and this ***should*** be capable of at least 10/100 mode.

2.6.1 Gb Ethernet Signal Definitions

The LAN interface of the COM Express Module consists of 4 pairs of low voltage differential pair signals designated from *'GBE0_MDI0'* (+ and -) to *'GBE0_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect to a 10/100/1000BASE-T RJ45 connector with integrated or external isolation magnetics on the Carrier Board. The corresponding LAN differential pair and control signals can be found on rows A and B of the Module's connector.

Table 18: Gb Ethernet Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
GBE0_MDI0+ GBE0_MDI0-	A13 A12	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used.	I/O GBE	
GBE0_MDI1+ GBE0_MDI1-	A10 A9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used	I/O GBE	
GBE0_MDI2+ GBE0_MDI02	A7 A6	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI2+/- N/C if not used.	I/O GBE	

<table>
<tr><th>Signal</th><th>Pin#</th><th>Description</th><th>I/O</th><th>Note</th></tr>
<tr><td>GBE0_MDI3+
GBE0_MDI3-</td><td>A3
A2</td><td>Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.
Module has integrated termination.
Carrier Board:
Connect to Magnetics Module MDI3+/-
N/C if not used</td><td>I/O GBE</td><td></td></tr>
<tr><td>GBE0_CTREF</td><td>A14</td><td>Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.
Carrier Board:
0.1uF to ground.
N/C if not used.</td><td>REF
GND min
3.3V max</td><td>1</td></tr>
<tr><td>GBE0_LINK#</td><td>A8</td><td>Ethernet controller 0 link indicator, active low.
Carrier Board:
N/C if not used.</td><td>O 3.3V
Suspend / 3.3V
OD CMOS</td><td></td></tr>
<tr><td>GBE0_LINK100#</td><td>A4</td><td>Ethernet controller 0 100Mbit/sec link indicator, active low.
Carrier Board:
N/C if not used.</td><td>O 3.3V
Suspend / 3.3V
OD CMOS</td><td></td></tr>
<tr><td>GBE0_LINK1000#</td><td>A5</td><td>Ethernet controller 0 1000Mbit/sec link indicator, active low.
Carrier Board:
N/C if not used.</td><td>O 3.3V
Suspend / 3.3V
OD CMO</td><td></td></tr>
<tr><td>GBE0_ACT#</td><td>B2</td><td>Ethernet controller 0 activity indicator, active low.
Carrier Board:
N/C if not used.</td><td>O 3.3V
Suspend / 3.3V
OD CMO</td><td></td></tr>
<tr><td>GBE0_SDP</td><td>A49</td><td>Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.</td><td>I/O
3.3V
Suspend / 3.3V</td><td></td></tr>
<tr><td>GBE0_MDI[0:3]+
GBE0_MDI[0:3]-</td><td></td><td>Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:
<table>
<tr><td></td><td>1000BASE-T</td><td>100BASE-TX</td><td>10BASE-T</td></tr>
<tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr>
<tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr>
<tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr>
<tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr>
</table></td><td>I/O
Analog</td><td></td></tr>
</table>

Note

2.6.2 SDP Pins

The Software Defined Pins (SDP) can be used to provide a timing communication path between the Module and Carrier. A board level signal that communicates time is a key element that facilitates clock synchronization between elements of a platform. Examples of such elements include, but are not limited to, CPU, Chipset, FPGA and others.

Modules ***should*** connect the SDP signal to a module element pin capable of propagating (transmitting) time, and/or time-stamping (receiving) the signal to extract time information from it. If implemented, the direction of the signal with respect to the module element ***should*** be able to be determined by system software.

Pulse Per Second (PPS):

A PPS signal conveys both frequency and phase and can be used to transfer time information between elements within a platform. It is commonly used because it encapsulates both frequency and time into a single signal. It is preferred over other methods that require more complex implementations of hardware and software. A GPS is probably the most widespread, high-quality, clock source capable of generating a PPS signal.

Platform-level Synchronization Implementation Examples:

Example1: The Network Interface Controller (NIC) on the COM Module is Precision Time Protocol (PTP) capable and the COM designer has connected a software configurable, timing aware, pin on the NIC to the SDP pin on the module/carrier interface. Software can configure the NIC to output a PPS signal onto this pin that connects it to one or more elements on the module and/or carrier board.

Example2: The carrier board has provisions for connecting a PPS output from a GPS to the SDP signal connection to the module. The module element (i.e. NIC, CPU, Chipset) can receive the timing information from the carrier board and adjust its time accordingly.

Precision Time Protocol - Background

Standards such as IEEE 1588, 802.1AS, and Time Sensitive Networking (TSN) provide standards for synchronizing time between nodes on a local area network. Additional benefits of the standards may include lower latency and improved network traffic Quality of Service (QoS). Systems that commonly require synchronization include those made up of distributed nodes that perform measurement, control, and compute functions. These nodes may have clock sources with varying degrees of accuracy and stability.

System-wide time synchronization with sub-microsecond accuracy is supported, by PTP standards, with minimal network and compute resource utilization.

It is the merger of the platform-level synchronization and network level synchronization pieces that enable real-time distributed systems. Additional information regarding the aforementioned standards can be found in their respective specifications and widely available supporting documents.

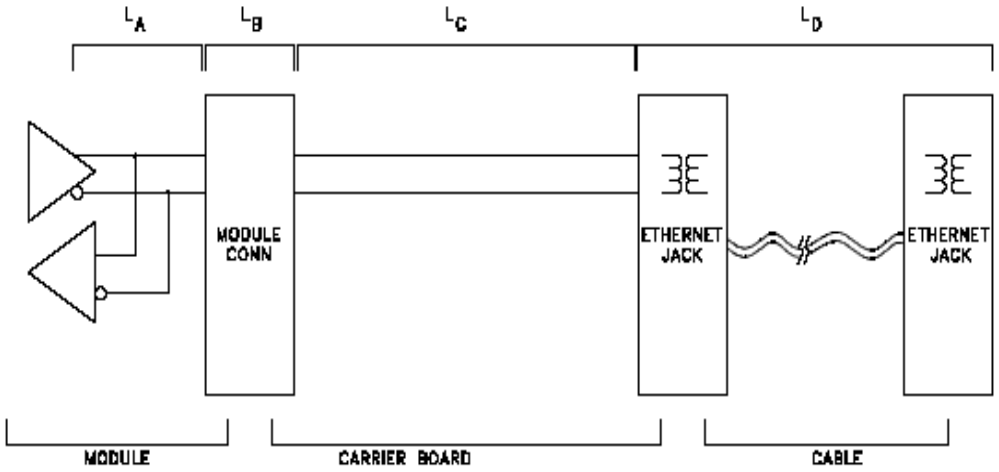
Software Implementation:

The software architecture and features required to support platform and network level synchronization are outside the scope of this specification.

2.6.3 Gb Ethernet Routing Guidelines

10/100/1000 Ethernet Insertion Loss Budget

Figure 16: 10/100/1000 Ethernet Insertion Loss Budget



COM Express Ethernet implementations should conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gb Ethernet specification.

“Device Down” implementations, in which the Ethernet target device is implemented on the Carrier Board (for instance, an Ethernet switch), may add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the Carrier Board budget. This insertion loss value is typically 1 dB. The Carrier Board insertion loss budget then becomes LC + 1 dB, or 1.15 dB.

Table 19: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.02	COM Express™ connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

2.6.4 Gb Ethernet Trace Length Guidelines

Figure 17: Topology for Ethernet Jack

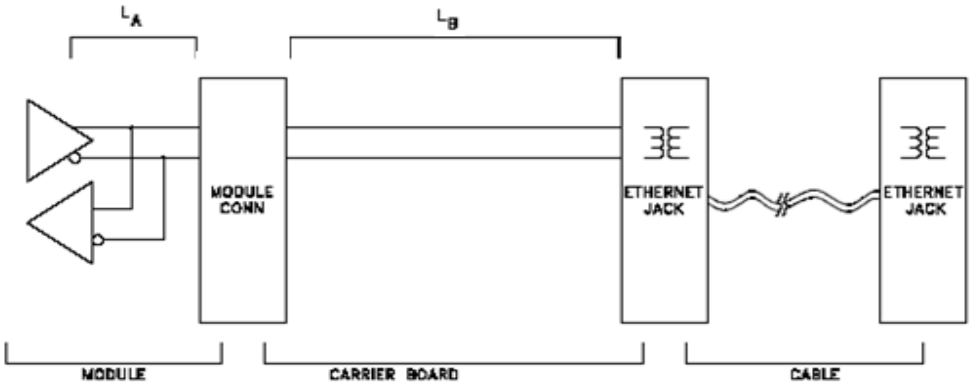


Table 20: Ethernet Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	GBE0_MDIx+, GBE0_MDIx-	
Differential Impedance Target	100 Ω ±10%	
Single End	55Ω ±10%	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils	
Spacing between differential pairs and high-speed periodic signals	Min. 300mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils	
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length;	
Max length of LA+LB	COM Express Module to the magnetics Module - 5.0 inches. Magnetics Module to RJ45 connector - Max. 1.0 inches.	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	
Reference Plane	GND referencing preferred..	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias.	

Notes:

2.6.5 Reference Ground Isolation and Coupling

The Carrier Board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier's digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the Carrier Board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

2.7 USB2.0 Ports

All USB interfaces ***shall*** be USB 2.0 compliant. The minimum of 4 USB channels provides support for keyboard, mouse, CD/DVD drive, and one additional device. Up to four USB 2.0 ports ***may*** support the extended signaling for SuperSpeed USB 3.0. USB0 ***may*** optionally be configured as a USB client.

2.7.1 USB2.0 Signal Definitions

Table 21: USB Signal Descriptions

Signal	Pin#	Description	I/O	Note
USB0+ USB0-	A46 A45	USB0 ***may*** be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, ***shall*** be host ports. USB Port 0, data + or D+ USB Port 0, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB1+ USB1-	B46 B45	USB Port 1, data + or D+ USB Port 1, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB2+ USB2-	A43 A42	USB Port 2, data + or D+ USB Port 2, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	

Signal	Pin#	Description	I/O	Note
USB3+ USB3-	B43 B42	USB Port 3, data + or D+ USB Port 3, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_0_1_OC#	B44	USB over-current sense, USB channels 0 and 1. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board. Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V SUSPEND / 3.3V CMOS	
USB_2_3_OC#	A44	USB over-current sense, USB channels 0 and 1. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board. Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V SUSPEND / 3.3V CMOS	
USB0_HOST_PRSNT	B48	Module USB client ***may*** detect the presence of a USB host on USB0. A high value indicates that a host is present. Carrier Board: N/C if not used	I 3.3V SUSPEND / 3.3V CMOS	1

Notes:

1. SOM-5992 is NC pin.

2.7.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, unconnected.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB overcurrent protection and therefore can be used as a replacement for power distribution switches.
Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

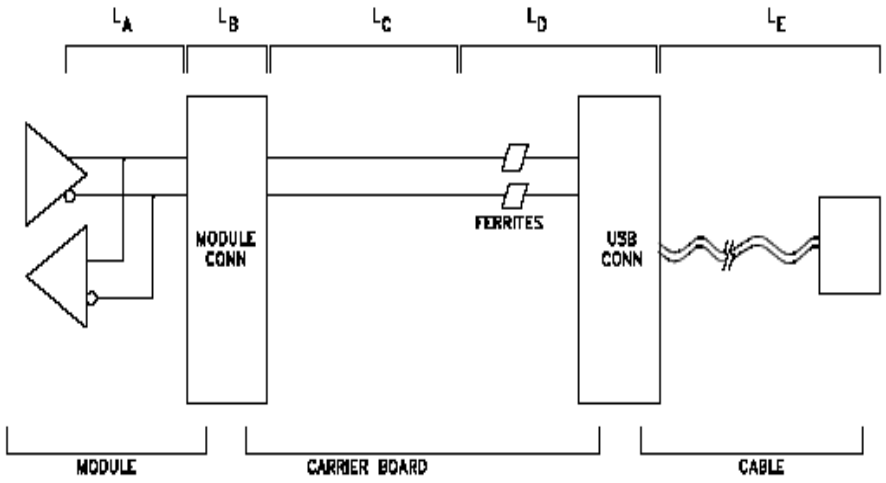
2.7.1.2 Powering USB devices during S5

The power distribution switches and the ESD protection shown in the schematics can be powered from Main Power or Suspend Power (VCC_5V_SBY). Ports powered by Suspend Power are powered during the S3 and S5 system states. This provides the ability for the COM Express Module to generate system wake-up events over the USB interface.

2.7.2 USB2.0 Routing Guidelines

USB 2.0 Insertion Loss Budget

Figure 18: USB 2.0 Insertion Loss Budget



COM Express USB implementations should conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, may add the ferrite and USB connector insertion loss values to the Carrier Board budget.

The Carrier Board insertion loss budget then becomes LC + LD, or 2.68 dB.

Table 22 :USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.05	COM Express connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

2.7.2.1 USB 2.0 General Design Considerations and Optimization

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems.

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential-pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20 x h rule by keeping traces at least [20 x (height above the plane)] mils away from the edge of the plane (VCC or GND). For an example stackup, the height above the plane is 4.5 mils (0.114 mm). This calculates to a 90-mil (2.286-mm) spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.
- Avoid stubs on high-speed USB signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils (5.08 mm).

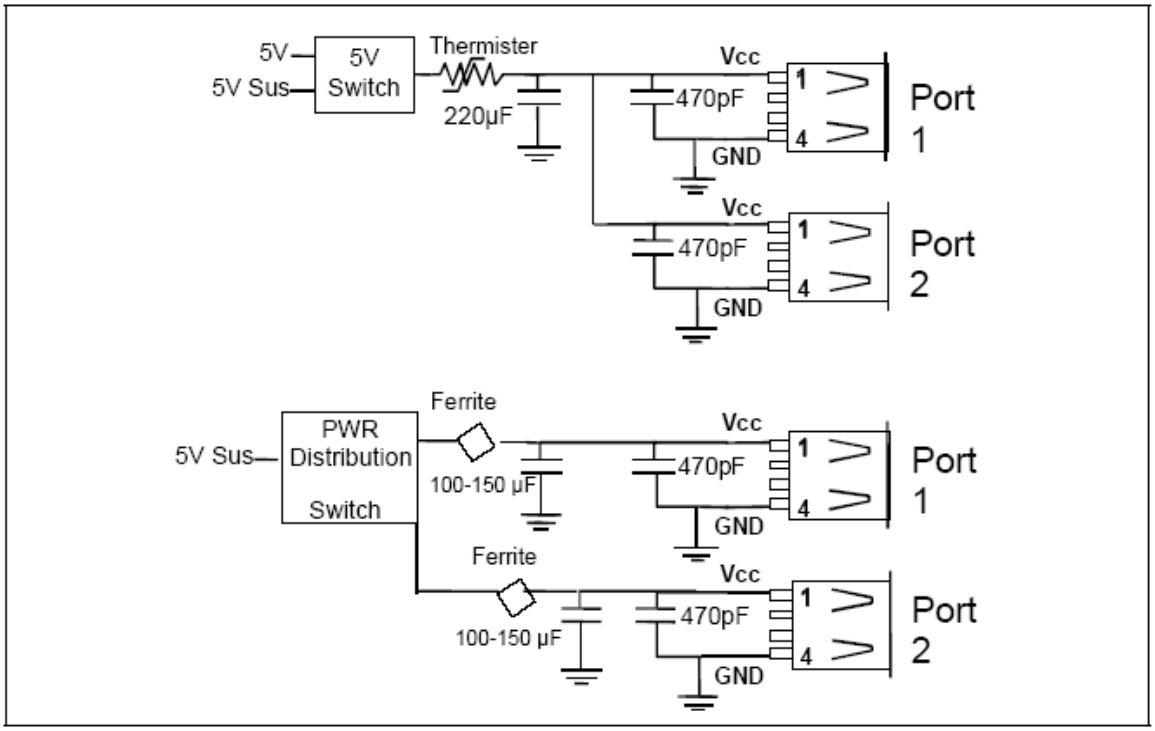
2.7.2.2 USB 2.0 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports.

These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.
- Make the power-carrying traces wide enough that the system fuse blows on an over current event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

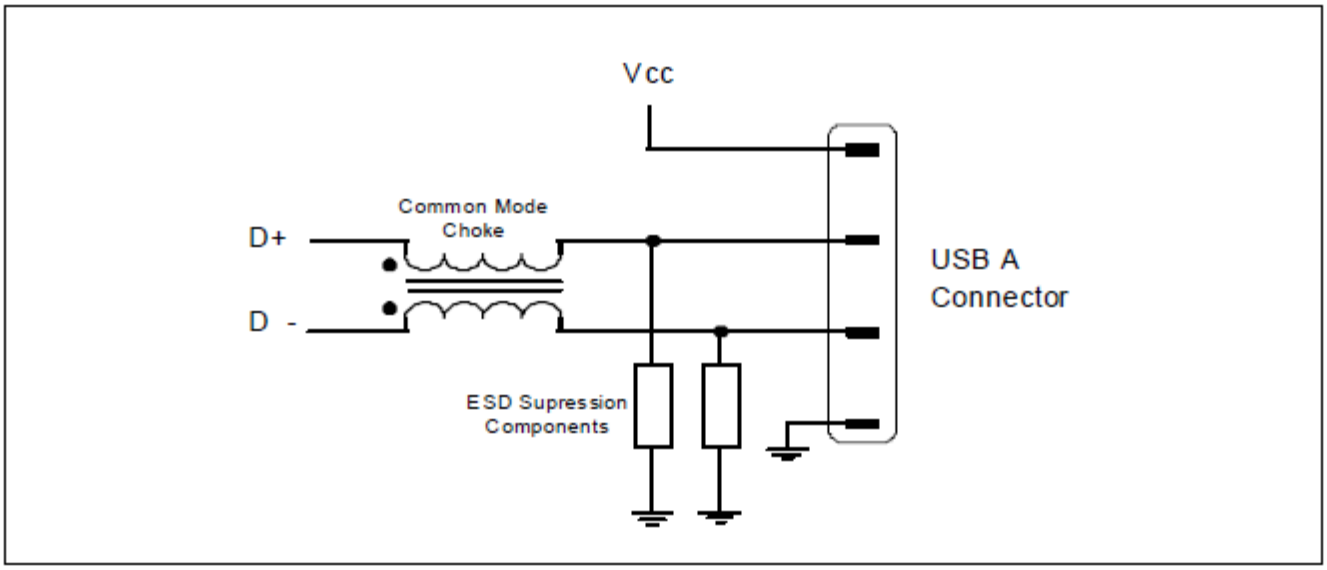
Figure 19: USB 2.0 Good Downstream Power Connection



2.7.2.3 USB 2.0 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins.

Figure 20: USB 2.0 A Common Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, therefore test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω, at 100 MHz, generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

1. Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that should be suppressed.
2. After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and highspeed USB operation.

Further common mode choke information can be found on the high-speed USB Platform Design Guides available at www.usb.org.

2.7.2.4 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.
Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design. In the USB reference schematics Figure 29 above, this is implemented by using 'SR05 RailClampR' surge rated diode arrays from Semtech (http://semtech.com).

2.7.3 USB2.0 Trace Length Guidelines

Figure 21: Topology for USB2.0

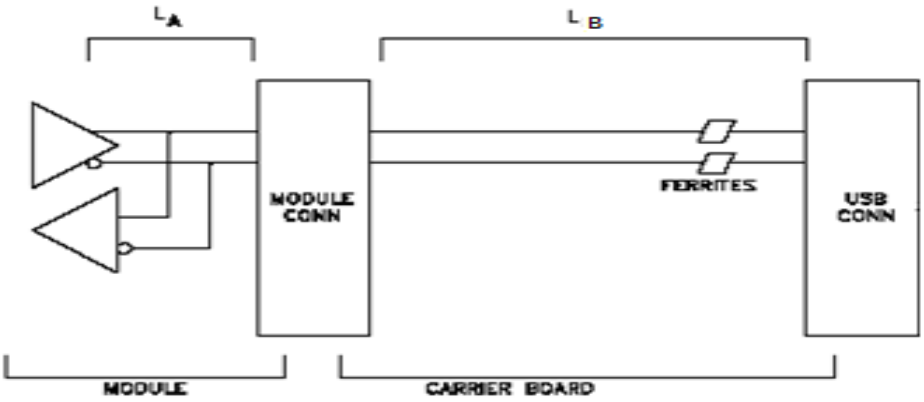


Table 23: USB2.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB[3:0]+, USB[3:0]-	
Differential Impedance Target	85 Ω ±10%	
Single End	55Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	7H (MS) and 5H (DS)	1
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	7H (MS) and 5H (DS)	1
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	16”	
Length matching	Differential pairs (intra-pair): Max. ±2 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Try to minimize number of vias	

Notes:

1. H is height above reference plane.

2.8 USB3.0

USB 3.0 is the third major revision of the Universal Serial Bus (USB) standard for computer connectivity. It adds a new transfer speed called SuperSpeed (SS) to the already existing LowSpeed (LS), FullSpeed (FS) and HighSpeed (HS).

USB 3.0 leverages the existing USB 2.0 infrastructure by adding two additional data pair lines to allow a transmission speed up to 5 Gbit/s, which is 10 times faster than USB 2.0 with 480 Mbit/s.

The additional data lines are unidirectional instead of the bidirectional USB 2.0 data lines. USB 3.0 is fully backward compatible to USB 2.0. USB 3.0 connectors are different from USB 2.0 connectors. The USB 3.0 connector is a super set of a USB 2.0 connector, with 4 additional pins that are invisible to USB 2.0 connectors. A USB 2.0 Type A plug may be used in a USB 3.0 Type A receptacle, but the USB 3.0 SuperSpeed functions will not be available.

2.8.1 USB3.0 Signal Definitions

Table 24: USB3.0 Signal Definitions

Signal	Pin#	Description	I/O	Note
USB_SSTX0+ USB_SSTX0-	D4 D3	USB Port 0, SuperSpeed TX + USB Port 0, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	
USB_SSTX1+ USB_SSTX1-	D7 D6	USB Port 1, SuperSpeed TX + USB Port 1, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	

Signal	Pin#	Description	I/O	Note
USB_SSTX2+ USB_SSTX2-	D10 D9	USB Port 2, SuperSpeed TX + USB Port 2, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	
USB_SSTX3+ USB_SSTX3-	D13 D12	USB Port 3, SuperSpeed TX + USB Port 3, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	
USB_SSRX0+ USB_SSRX0-	C4 C3	USB Port 0, SuperSpeed RX + USB Port 0, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	

Signal	Pin#	Description	I/O	Note
USB_SSRX1+ USB_SSRX1-	C7 C6	USB Port 1, SuperSpeed RX + USB Port 1, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	
USB_SSRX2+ USB_SSRX2-	C10 C9	USB Port 2, SuperSpeed RX + USB Port 2, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	
USB_SSRX3+ USB_SSRX3-	C13 C12	USB Port 3, SuperSpeed RX + USB Port 3, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	

Notes:

2.8.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, unconnected.

Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

USB 2.0 port's VCC current limit should be set to 500mA. For USB 3.0 implementations, the VCC current limit is raised to 1A. A different, USB 3.0 compatible, power switch is used.

2.8.1.2 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.

Common mode chokes can provide required noise attenuation but they also distort the signal quality of FullSpeed, HighSpeed and SuperSpeed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.8.2 USB3.0 Routing Guidelines

USB3.0 Insertion Loss Budget

Figure 22: USB3.0 Insertion Loss Budget

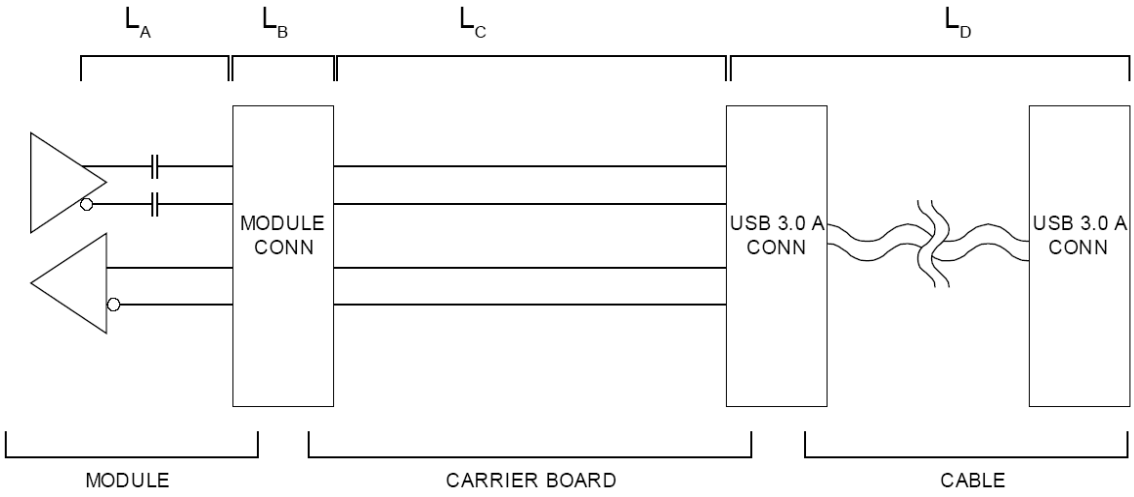


Table 25: USB3.0 Insertion Loss Budget

Segment	Loss (dB)	Notes
L_A	1.94	Up to 3 inches of Module trace @ 2.5 GHz
L_B	1.20	COM Express connector at 2.5 GHz
L_C	3.64	Up to 5 inches of Carrier Board trace @ 2.5 GHz with Common-Mode Component
Total	6.78	

2.8.3 USB3.0 Trace Length Guidelines

Figure 23: Topology for USB3.0

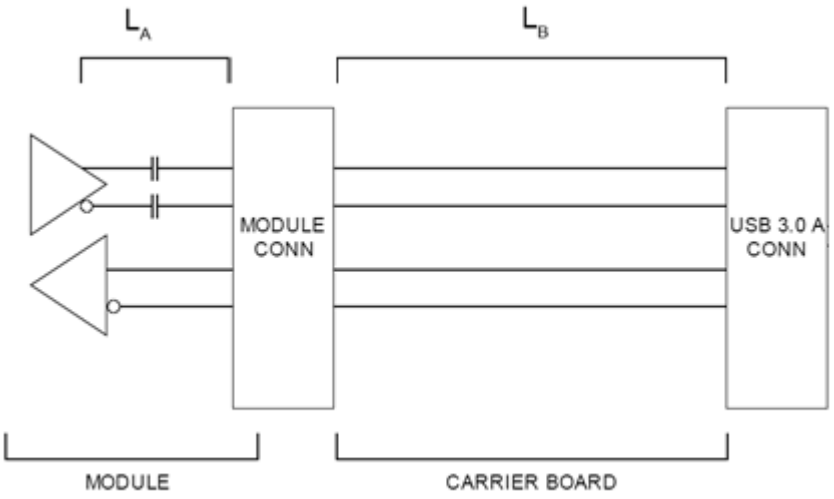


Table 26: USB3.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB3.0	
Differential Impedance Target	85Ω ±10%	
Single End	55Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	9H (MS) and 5H (DS)	1, 2
Spacing between differential pairs and high-speed periodic signals	11H (MS) and 7H (DS)	1
Spacing between differential pairs and low-speed non periodic signals	11H (MS) and 7H (DS)	1
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	10”	
Length matching	Differential pairs (intra-pair): Max. ±2 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 3 vias per differential signal trace	

Notes:

1.H is height above reference plane.

2.Spacing pairs to pairs are TX to TX or RX to RX(Noninterleaved)

2.9 SATA

Support for up to two SATA ports is defined on the COM Express A-B connector. Support for a minimum of 0 port is required for Module Type 7. Serial ATA links for support of existing SATA-150 (revision 1.0, 1.5Gb/s), SATA-300 (revision 2.0, 3Gb/s), and SATA-600 (revision 3.0, 6Gb/s) devices. The COM Express Specification addresses both in the section on insertion losses.

SATA devices can be internal to the system or external. The eSATA specification defines the connector used for external SATA devices. The eSATA interface must be designed to prevent damage from ESD, comply with EMI limits, and withstand more insertion/removals cycles than standard SATA. A specific eSATA connector was designed to meet these needs. The eSATA connector does not have the "L" shaped key, and because of this, SATA and eSATA cables cannot be interchanged.

2.9.1 SATA Signal Definitions

Table 27: SATA Signal Definitions

Signal	Pin#	Description	I/O	Note
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 6 RX+ Connect to SATA0 Conn pin 5 RX- N/C if not used.	I SATA	
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit output differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 2 TX+ Connect to SATA0 Conn pin 3 TX- N/C if not used.	O SATA	
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA1 Conn pin 6 RX+ Connect to SATA1 Conn pin 5 RX- N/C if not used.	I SATA	

Signal	Pin#	Description	I/O	Note
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit output differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA1 Conn pin 2 TX+ Connect to SATA1 Conn pin 3 TX- N/C if not used.	O SATA	
SATA_ACT#	A28	Serial ATA activity LED. Open collector output pin driven during SATA command activity. Module has integrated PU resistor Carrier Board: Connect to LED and current limiting resistors 250 to 330 Ω to 3.3V N/C if not used.	I/O 3.3V CMOS	Able to drive 10 mA

Notes:

2.9.2 SATA Routing Guidelines

SATA Insertion Loss Budget

The Serial ATA source specification provides insertion loss figures only for the SATA cable.

There are several cable types defined with insertion losses ranging from 6 dB up to 16 dB.

Cross talk losses are separate from material losses in the SATA specification.

The COM Express SATA Insertion loss budgets presented below represent the material losses and do not include cross talk losses. The COM Express SATA Insertion loss budgets are a guideline: Module and Carrier Board vendors ***should not*** exceed the values shown in the tables below.

Figure 24: SATA Insertion Loss Budge

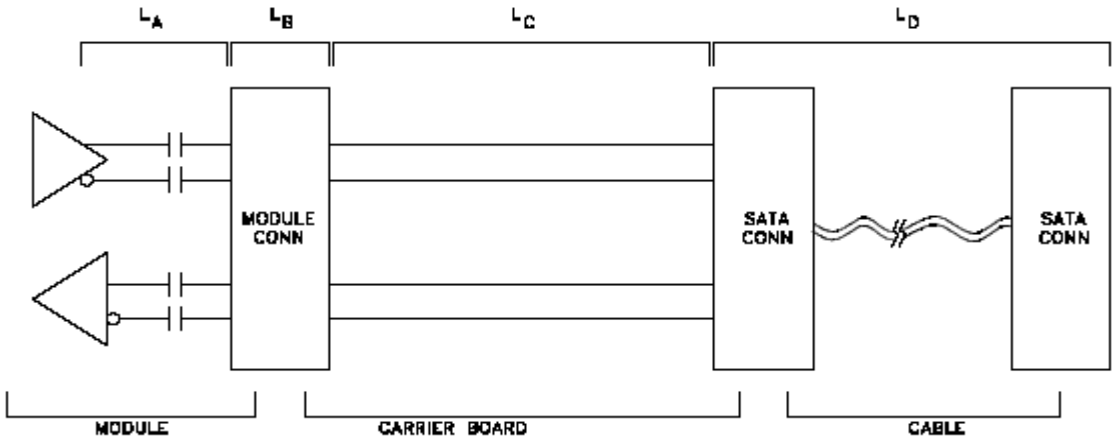


Table 28: SATA Insertion Loss Budge

SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	COM Express™ connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	COM Express™ connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

2.9.2.1 General SATA Routing Guidelines

Use the following general routing and placement guidelines when laying out a new design.

- SATA signals must be ground referenced. If changing reference plane is completely unavoidable (that is, ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are smallvalued capacitors (1 µF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created. The maximum number allowed for SATA to change reference plane is one.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided.
- Minimize layer changes. If a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Intel recommends to use SATA vias as seldom as possible.
- **DO NOT** route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- **DO NOT** place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead.

- For testability, route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Length matching rules are required on SATA differential signals for optimum timing margins, preventing common-mode signals and EMI.Each net within a differentialpair should be length matched on a segment-by-segment basis at the point of discontinuity. Total length mismatch must not be more than 20 mils (0.508 mm). Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity would be the via, the capacitor pad, or the connector pin.Matching of TX and RX within the same port and between SATA TX and RX pairs from differential ports is not required. When length matching compensation occurs, it should be made as close as possible to the point where the variation occurs.
- **DO NOT** serpentine to match RX and TX traces; there is **NO** requirement to match RX and TX traces. In addition, **DO NOT** serpentine to meet minimum length guidelines on RX and TX traces.
- Recommend keeping SATA traces 20 mils (0.508 mm) from any vias on the motherboard whenever possible.

2.9.3 SATA Trace Length Guidelines

Figure 25: Topology for SATA

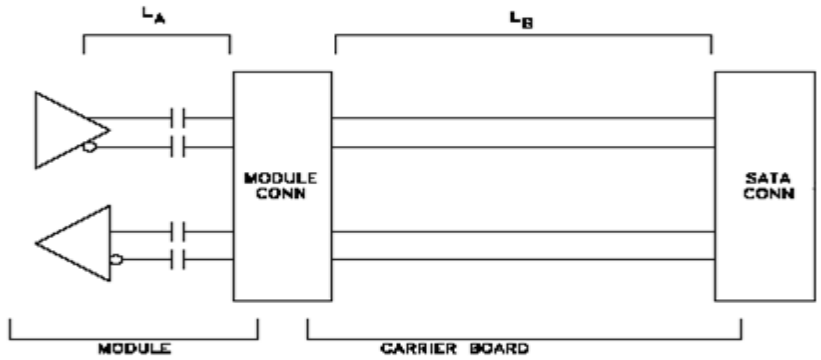


Table 29: SATA Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SATA	
Differential Impedance Target	85 Ω ±10%	
Single End	50~55Ω ±15%	
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates	
Spacing between RX and TX pairs (inter-pair) (s)	9H (MS) and 7H (DS)	1
Spacing between differential pairs and high-speed periodic signals	9H (MS) and 7H (DS)	1
Spacing between differential pairs and low-speed non periodic signals	9H (MS) and 7H (DS)	1
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	Support Gen3 : “2~5”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	A maximum of 2 vias is recommended.	
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module.	

Notes:

1.H is height above reference plane.

2.10 LPC and eSPI Interface *SOM-5992 is not support eSPI.

The Module LPC and eSPI interfaces share connector pins. A Module design ***may*** support either LPC or eSPI or both, at the Module vendor's discretion. Module pin ESPI_EN# is available for the Carrier to signal to the Module whether LPC or eSPI is to be used. The Carrier ***shall*** leave the ESPI_EN# unconnected on the Carrier for LPC operation. The Carrier ***shall*** tie ESPI_EN# to GND for eSPI operation. The Module ***shall*** terminate ESPI_EN# as appropriate to facilitate this.

The LPC bus is a 3.3V bus and eSPI is a 1.8V bus. There is the possibility of a mismatch – an eSPI only Module mated with a LPC only Carrier, or an LPC only Module on an eSPI Carrier. Module designers ***should*** protect the Module eSPI interface against accidental exposure to 3.3V Carrier LPC signals. Carrier designers ***should*** protect a Carrier eSPI interface against accidental exposure to 3.3V Module LPC signals. In both cases, a simple and low cost protection scheme ***may*** be realized with low value in-line series resistors (typically 33 ohms) and BAT54 Schottky diodes on each line. The diode anode is tied to the eSPI device pin and the cathode to the 1.8V supply rail. Ideally, that 1.8V supply rail can sink current. In the event of a mismatch, the offending (Module or Carrier) 3.3V rail is discharged through the series resistor and the Schottky diode to the (Carrier or Module) 1.8V rail and not through the eSPI device.

2.10.1 LPC /eSPI Signal Definition

Table 30: LPC/eSPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
LPC_SERIRQ	A50	LPC serialized IRQ. Carrier Board: Connect to LPC - SERIRQ N/C if not used	I/O 3.3V CMOS	
ESPI_CS1#		ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. Carrier Board: Connect to eSPI Device – eSPI_CS1# N/C if not used	O 1.8V Suspend / 1.8V	2

Signal	Pin#	Description	I/O	Note
LPC_FRAME#	B3	LPC frame indicates start of a new cycle or termination of a broken cycle. Carrier Board: LPC - LFRAME# N/C if not used	O 3.3V CMOS	
ESPI_CS0#		ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. Carrier Board: Connect to eSPI Device – eSPI_CS0# N/C if not used	O 1.8V Suspend / 1.8V	2
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed command, address and data. Carrier Board: Connect to LPC - LAD0 , LAD1, LAD2, LAD3 N/C if not used	I/O 3.3V CMOS	
ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3		ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. Multiplexed with LPC_AD[0:3] Carrier Board: Connect to eSPI Device – eSPI_IO0, eSPI_IO1, eSPI_IO2, eSPI_IO3, the Carrier ***shall*** have a 33 Ohm series termination. N/C if not used	I/O 1.8V Suspend / 1.8V	2
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC encoded DMA/Bus master request. Carrier Board: Connect to LPC - LDRQ0#, LDRQ1# N/C if not used	I 3.3V CMOS	Not all Modules support LPC DMA. Contact your vendor for information.
ESPI_ALERT0# ESPI_ALERT1#		ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master. Carrier Board: Connect to eSPI Device – eSPI_ALERT0#, eSPI_ALERT1#. N/C if not used	I 1.8V Suspend / 1.8V	2

Signal	Pin#	Description	I/O	Note
ESPI_RESET# /SUS_STAT#	B18	ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves. Carrier Board: Connect to eSPI Device – eSPI_RESET# N/C if not used	O 1.8V Suspend / 1.8V	2
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic **high** on the module through a resistor. The Carrier ***should*** only float this line or **pull it low**. Carrier Board: Connect to N/C : LPC mode GND: eSPI mode	I NA CMOS	2
LPC_CLK	B10	LPC clock output 24MHz. Carrier Board: Connect to LPC - LCLK N/C if not used	O 3.3V CMOS	
ESPI_CK		ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations. Carrier Board: Connect to eSPI Device – eSPI_CLK, the Carrier ***shall*** have a 33 Ohm series termination. N/C if not used	O 1.8V Suspend / 1.8V	2

Note:

1. Implementing external LPC devices on the COM Express Carrier Board always requires customization of the COM Express Module's BIOS in order to support basic initialization for those LPC devices. Otherwise the functionality of the LPC devices will not be supported by a Plug&Play or ACPI capable system.

2. SOM-5992 is not support eSPI.

2.10.2 LPC Routing Guidelines

2.10.2.1 General Signals

LPC signals are similar to PCI signals and may be treated similarly. Route the LPC bus as 50 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching among LPC_AD[3:0], LPC_FRAME# are needed

2.10.2.2 Bus Clock Routing

Route the LPC clock as a single-ended, 50 Ω trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground referenced internal layer is preferred to reduce EMI.

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the COM Express specification and the 'PCI Local Bus Specification Revision 2.3'.

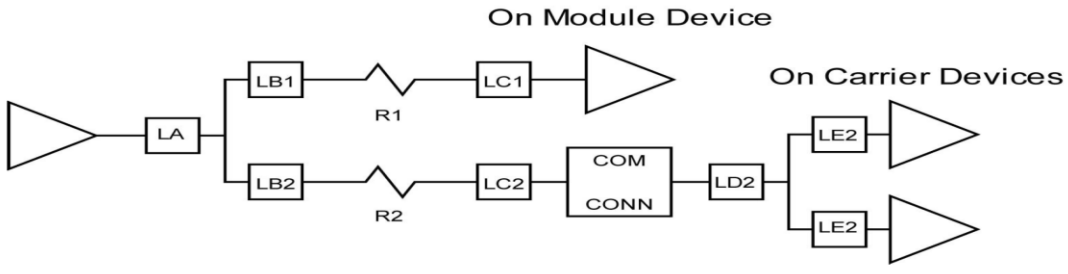
2.10.2.3 Carrier Board LPC Devices

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads ***should*** be connected to the common clock without a buffer. The Carrier Board ***should*** not have more than two loads on the LPC clock.

Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 26: Typical routing topology for a Module LPC device



LA 500 mils max
LB1 = LB2 = 150 mils max
LC1 = 8.88”+LC2
LC2 = .25” max
LE2 = 1” max
LD2 + LE2 (note 2 instances of LE2) = 8.88”
R1 = R2 = 22Ω

2.10.2.4 eSPI Devices

At the time of this writing, the use case and design rules for eSPI are still being developed.

Designers of Modules and Carriers are provided with the following guidance:

The maximum trace length for Carrier routed eSPI traces ***shall not*** exceed 4.5”.

Carrier routed ESPI traces ***shall*** be routed at 50 Ohms.

Carrier routed SPI traces ***shall*** have 5 mil via to via clearance, 4 mil trace to via clearance, and 10 mil clearance to any other traces.

The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_CK signal.

The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_IO_[0..3] signals.

The Carrier ***shall*** length match ESPI_CK and ESPI_IO_[0..3] within 250mils.

The Carrier ***shall*** length match eSPI_CK and ESPI_CS within 100mils.

2.10.3 LPC Trace Length Guidelines

Figure 27: Topology for LPC

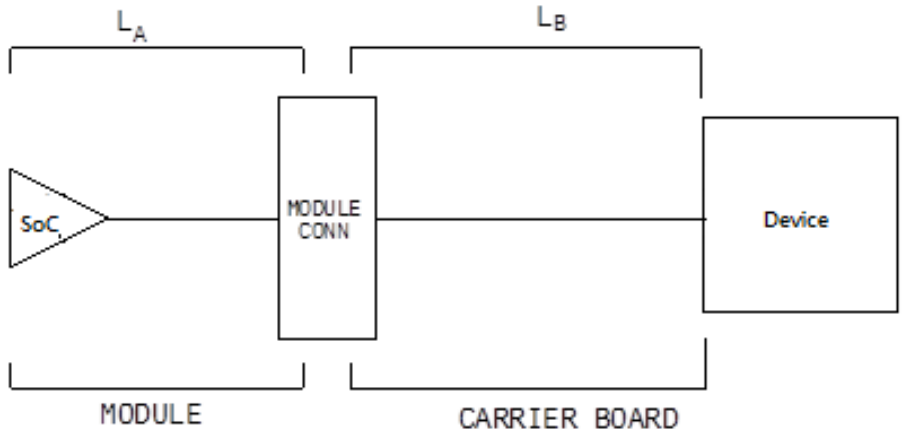


Table 31: LPC Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LPC	
Single End	50~55Ω ±10%	
Nominal Trace Space within LPC Signal Group	Min. 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	23”	
Length matching between single ended signals	Max. 250mils	
Length matching between clock signals	Max. 250mils	
Reference Plane	GND referencing preferred.	
Via Usage	Try to minimize number of vias	

Notes:

2.11 SPI – Serial Peripheral Interface Bus

The SPI bus is used to support SPI-compatible flash devices. The SPI flash device can be up to 16 MB (128 Mb). The SPI bus is clocked at either 20 MHz, 25 MHz, 33 MHz or 50 MHz. SPI devices selected ***should*** support one of these frequencies.
In COM.0 Rev 2, the SPI interface was defined as a 3.3V interface. With COM.0 Rev 3, the SPI interface ***may*** be either 3.3V or 1.8V, as is best for the Module chipset at hand.

2.11.1 SPI Signal Definition

Table 32: SPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SPI_CS#	B97	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1 Carrier Board: Connect to SPI flash pin 1 Chip Select N/C if not used	O CMOS 3.3V Suspend or 3.3V S0 1.8V Suspend or 1.8V S0	
SPI_MISO	A92	Data in to Module from Carrier SPI Carrier Board: Connect 15~33Ω in series to SPI flash pin 2 Serial Output N/C if not used	I CMOS 3.3V Suspend or 3.3V S0 1.8V Suspend or 1.8V S0	
SPI_MOSI	A95	Data out from Module to Carrier SPI Carrier Board: Connect 33~47 Ω in series to SPI flash pin 5 Serial Input N/C if not used	O CMOS 3.3V Suspend or 3.3V S0 1.8V Suspend or 1.8V S0	
SPI_CLK	A94	Clock from Module to Carrier SPI Carrier Board: Connect 33~47 Ω in series to SPI flash pin 6 Clock N/C if not used	O CMOS 3.3V Suspend or 3.3V S0 1.8V Suspend or 1.8V S0	

Signal	Pin#	Description	I/O	Note
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier. Carrier Board: Connect to SPI flash pin 8 VDD N/C if not used	O 3.3V Suspend or 3.3V S0 1.8V Suspend or 1.8V S0	
BIOS_DIS0# / ESPI_SAFS	A34	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to Table X: BIOS Selection Straps. Carrier Board: 1 - N/C 0 - PD 1K to GND	I CMOS	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to Table X: BIOS Selection Straps. Carrier Board: 1 - N/C 0 - PD 1K to GND	I CMOS	
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier ***should*** only float this line or **pull it low**. please refer to Table33: BIOS Selection Straps. Carrier Board: 1 - N/C 0 - PD 1K to GND	I CMOS	1

Note:

1. SOM-5992 is NC.

SPI Power

Introducing a SPI_POWER pin is desirable because some Module implementations will have the SPI power domain in power state S0 and others in S5. It is easier for Carrier Board designers to take the Carrier SPI power from a pin on the Module.

The SPI_POWER voltage level was defined as 3.3V in COM.0 Rev. 2. With COM.0 Rev. 3, the SPI_POWER voltage level ***may*** be 3.3V or 1.8V. This allows the Carrier SPI interface to operate at the level appropriate for the Module chipset, without the use of level shifters.

Module designs that implement a 1.8V Carrier SPI interface ***should*** protect themselves against possible exposure to 3.3V Carrier SPI signals.

Carrier designs that implement a 1.8V SPI interface ***should*** protect themselves against possible exposure to 3.3V Module SPI signals.

Module Vs Carrier Board Pull-ups

There ***shall*** not be any Carrier Board pull-ups or pull-downs on the five SPI_x signals. All such terminations ***shall*** be on the Module. The Module designer ***shall*** determine the correct power domain that these signals are terminated to.

Note: Carrier Board ***shall*** implement pull-ups to SPI_POWER on the SPI flash pins HOLD# and WP# which are not supported on the COM Express connector.

2.11.2 BIOS Boot Selection

For COM.0 R3, the Module Carrier based BIOS options have been expanded to support eSPI devices. A third pin that affects the BIOS location, named ESPI_EN#, works in conjunction with BIOS_DIS1# and BIOS_DIS0# to define the BIOS boot path. Additionally, the concepts of Master Attached Flash Sharing (MAFS) and Slave Attached Flash Sharing (SAFS) are introduced.
LPC bus BIOS FWH support is removed in COM.0 R3. SPI and eSPI BIOS options are supported.

SPI Boot Flash Background

Contemporary Intel x86 systems requires that the SPI boot flash to be divided into a number of regions that may include:

- Descriptor
- BIOS code
- Management Engine (ME) code
- GBE parameters
- Platform data

The Descriptor defines where the other regions are in the SPI device(s). The Descriptor is always at the bottom of the first SPI device, the SPI device that is selected by chipset SPI0 chip-select (chipset SPI_CS0#).
The first two regions, the Descriptor and the BIOS, are mandatory. The other regions are optional. The regions may all be packed into the same SPI device, or may be divided between more than one SPI device, although the Descriptor has to be at the bottom of the first SPI device. In most situations, all the SPI regions are packed into a single SPI device that is either on the Module or on the Carrier. Designers may have reasons for dividing the SPI boot flash regions between devices.
COM Express Rev 2 and Rev 3 define a SPI interface on the COM Express connector. The COM Express SPI interface has only one chip select. Chipsets typically have 2 SPI chip selects. Module hardware may steer those chipset chip selects to an on-Module SPI device or devices or to a single off-module SPI device. The chip select steering is defined by the ESPI_EN#, BIOS_DIS1# and BIOS_DIS0# signals.‘BIOS Selection Straps‘ below.

The BIOS Entry point *may* be in SPI0 or SPI1 as determined by the descriptor table in the SPI0 device. The Module *may* have one or two SPI devices. Carrier Boards *may* have zero or one SPI devices.

MAFS and SAFS BIOS Configurations

Master Attached Flash Sharing (MAFS) is defined as the BIOS Flash directly attached to the processor SPI bus.

Slave Attached Flash Sharing (SAFS) is defined as the BIOS Flash being attached behind a board Management Controller (BMC) or Embedded Controller (EC).

MAFS and SAFS configurations apply to both LPC and eSPI enabled configurations. Refer to Figure27 'BIOS Selection LPC Mode' and Figure28 'BIOS Selection eSPI Mode' below.

Please note that some of the features shown in these figures are mutually exclusive.

Figure 28: BIOS Selection LPC Mode

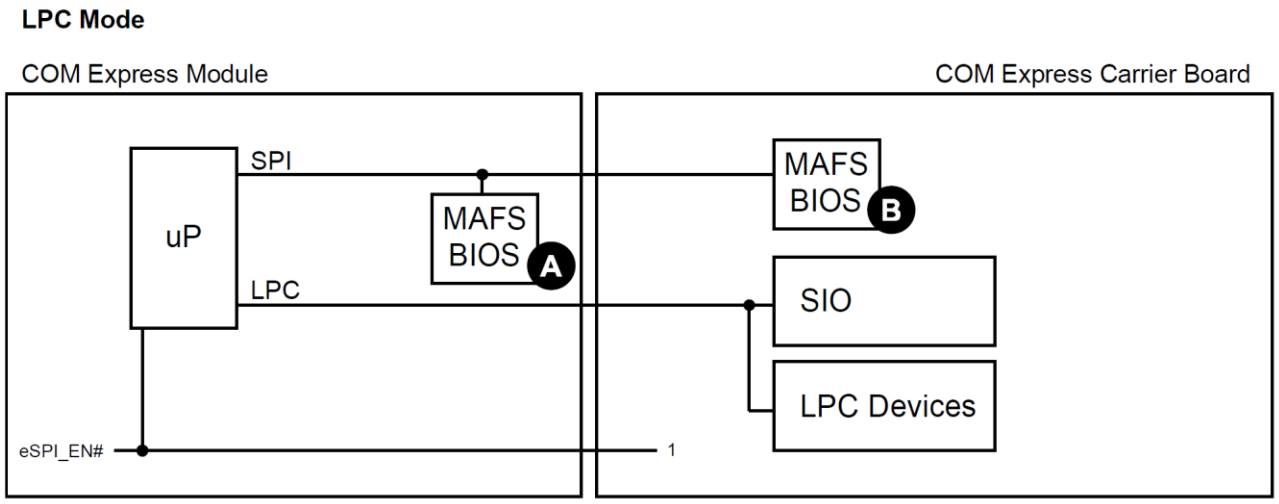
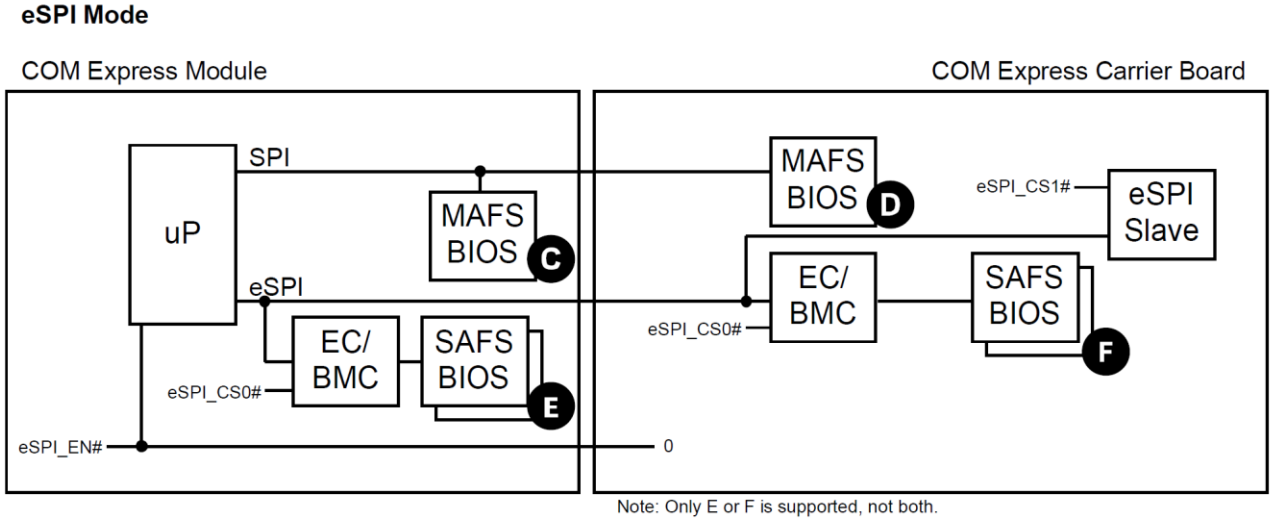


Figure 29: BIOS Selection eSPI Mode



Note: Only E or F is supported, not both.

The A and, B notations in the figure26 above and the B, C, D and F notations in figure27 above are referenced in the table and text sections below. Note also that some of the features shown in these figures are mutually exclusive.

Table 33: BIOS Selection Straps

ESPI_EN#	BIOS_DIS1#	BIOS_DIS0#	Boot Bus	BBS	Chipset ESPI_CS0# Destination	Carrier ESPI_CS0# Pin	Chipset SPI_CS1# Destination	Chipset SPI_CS0# Destination	Carrier SPI_CS# Pin	SPI Descriptor	Ref to Images Above	Notes
1	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	A	MAFS on Module. LPC bus enabled.
1	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	B	MAFS on Carrier. LPC bus enabled.
1	1	0	-	0	-	-	-	-	High	-	-	Not used - was FWH
1	1	1	SPI	0	-	-	Module	Module	High	Module	A	MAFS on Module. LPC bus enabled.
0	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	C	MAFS on Module. ESPI bus enabled.
0	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	D	MAFS on Carrier. ESPI bus enabled.
0	1	0	eSPI	1	Module	-	-	-	SPI0	Module	E	SAFS and BMC on Module. ESPI bus enabled.
0	1	1	eSPI	1	Carrier	Chipset ESPI_CS0#	-	-	SPI0	Carrier	E	SAFS and BMC on Carrier. ESPI bus enabled.

The BBS (BIOS Boot Select) is a signal to the chipset that indicates if the system is using a MAFS (Master Attached File Sharing) or SAFS (Slave attached File Sharing) setup. The BBS signal ***may*** be formed by Module logic looking for ESPI_EN# low and BIOS_DIS1# high.

The ESPI_CS1# line is not used for BIOS boot functions; it may be used to attach a secondary slave device to the eSPI bus, if the chip select is available.

SPI BIOS MAFS Considerations – LPC Enabled

The first four lines in Table 33 above are backwards compatible with the SPI BIOS options described in COM.0 Rev. 2, except that LPC FWH support is removed in COM.0 Rev 3. The LPC bus is enabled and is available for use on the Module or the Carrier for peripheral devices such as Board Management Controllers (BMC), Embedded Controllers (EC), Super I/O (SIO) or other general purpose devices.

SPI BIOS MAFS Considerations – eSPI Enabled

In an eSPI enabled MAFS system, the BIOS flash is attached to the system SPI bus, either on-Module or off-Module, much as in the LPC enabled MAFS system described above. The eSPI bus replaces the LPC bus for use with peripheral devices such as BMCs, ECs, SIOs etc. but the BIOS boot path is on the SPI bus.

eSPI BIOS SAFS Considerations – eSPI Enabled

In an eSPI enabled SAFS system, the SPI boot device is located on the far side of a BMC or EC. The system can boot from either a Module SAFS (in Figure 27 above) or a Carrier SAFS (in Figure 27 above). The BIOS boot traffic is routed through the BMC or EC to the system eSPI bus and on to the chipset.

It is possible for both a Module and a Carrier SAFS to be present in a system, but only one can be enabled. This is accomplished by routing the ESPI_CS0# signal to the Module or the Carrier, but never both. This is by definition of the eSPI specification. A second ESPI_CS1# is available to select eSPI slave devices. Slave devices can be on the Module or the Carrier.

Two eSPI alert pins are provided. Additional alert pins are permitted by the eSPI specification through alert pin sharing on the EC/BMC or by signal tunneling.

2.11.3 SPI Routing Guidelines

NA

2.11.4 SPI Trace Length Guidelines

Figure 30: Topology for SPI

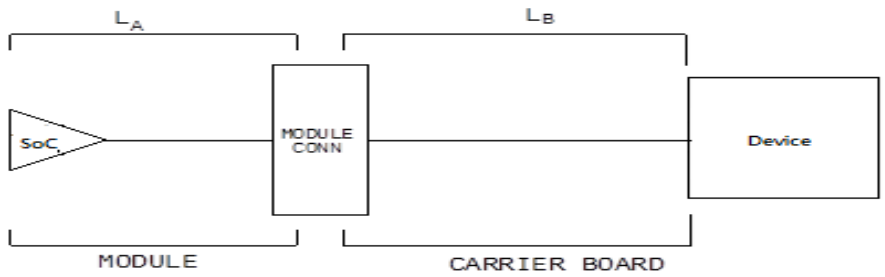


Table 34: SPI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SPI	
Single End	50Ω ±10%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 10mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	6.5”	
SPI CLOCK to MOSI and CLOCK to SPI_CS Maximum Pin to Pin Length Mismatch	Max. 500mils	
Via Usage	Try to minimize number of vias	

Notes:

2.12 General Purpose I2C Bus Interface

The I2C port ***shall*** be available in addition to the SMBus. The I2C clock ***shall*** support 100kHz and ***should*** support 400kHz operation. The maximum capacitance on the Carrier Board ***shall*** not exceed 100pF. The I2C interface ***should*** support multi-master operation. This capability will allow a Carrier to read an optional Module EEPROM before powering up the Module.

Revision 1.0 of the specification placed the I2C interface on the non-standby power domain. With this connection, the I2C interface can only be used when the Module is powered on. Since the I2C interface is used to connect to an optional Carrier EEPROM and since it is desirable to allow a Module based board controller access to the optional Carrier EEPROM before the Module is powered on, revision 3.x of this specification changes the power domain of the I2C interface to standby-power allowing access during power down and suspend states. There is a possible leakage issue that can arise when using a R3.x Module with a R2.1 Carrier that supports I2C devices. The R2.1 Carrier will power any I2C devices from the non-standby power rail. A R3.x Module will pull-up the I2C clock and data lines to the standby-rail through a 2.2K resistor. The difference in the power domains on the Module and Carrier can provide a leakage path from the standby power rail to the non-standby power rail.

2.12.1 Signal Definitions

The general purpose I2C Interface is powered from 3.3V suspend rail. The I2C_DAT is an open collector line with a pull-up resistor located on the Module. The I2C_CK has a pull-up resistor located on the Module. The Carrier should not contain pull-up resistors on the I2C_DAT and I2C_CK signals. Carrier based devices should be powered from 3.3V suspend voltage. The use of main power line for a Carrier I2C device will require a bus isolator to prevent leakage to other I2C devices on 3.3V power.

At this time, there is no allocation of I2C addresses between the Module and Carrier. Carrier designers will need to consult with Module providers for address ranges that can be used on the Carrier.

Table 35: General Purpose I2C Interface Signal Descriptions

Signal	Pin#	Description	I/O	Pwr Rail	Note
I2C_CK	B33	General Purpose I2C Clock output Carrier Board: 3.3VSB I2C device - Connect to SCL of I2C device. 3.3V I2C device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SCL of I2C device. 5VSB I2C device - Connect 5VSB Level Shifter to SCL of I2C device. 5V I2C device – Connect an 5V isolation circuit controlled by COME pin B24 PWR_OK to SCL of I2C device. N/C if not used	I/O OD CMOS	3.3V Suspend / 3.3V	
I2C_DAT	B34	General Purpose I2C data I/O line. Carrier Board: 3.3VSB I2C device - Connect to SDA of I2C device. 3.3V I2C device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SDA of I2C device 5VSB I2C device - Connect 5VSB Level Shifter to SDA of I2C device 5V I2C device - Connect an 5V isolation circuit controlled by COME pin B24 PWR_OK to SDA of I2C device N/C if not used	I/O OD CMOS	3.3V Suspend / 3.3V	

2.12.2 I2C Routing Guidelines

NA

2.12.3 I2C Trace Length Guidelines

Figure 31: Topology for I2C

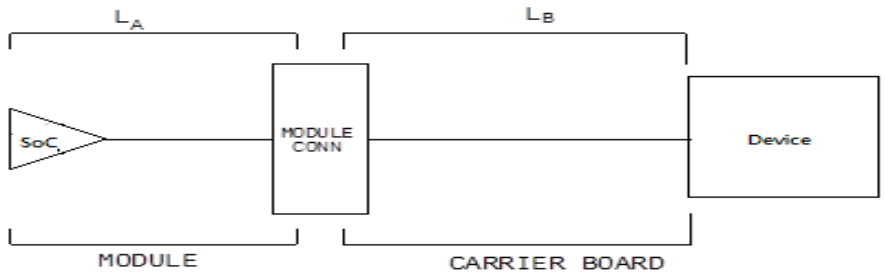


Table 36: I2C Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	I2C	
Single End	50Ω ±15%	
Nominal Trace Space within I2C Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 10mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	ASPA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.12.4 Connectivity Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by Advantech's Module. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 8pF of capacitance, and a PCB trace has 3.8pF per inch of trace length.

2.13 System Management Bus (SMBus)

The SMBus is primarily used as an interface to manage peripherals such as serial presence detect (SPD) on RAM, thermal sensors, PCIe devices, smart battery, etc. The devices that can connect to the SMBus can be located on the Module and Carrier. Designers need to take note of several implementation issues to ensure reliable SMBus interface operation. The SMBus is similar to I2C. I2C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition. Designers are urged to use SMBus devices when possible over standard I2C devices. COM Express Modules are required to power SMBus devices from Early Power in order to have control during system states S0-S5. The devices on the Carrier Board using the SMBus are normally powered by the 3.3V main power. To avoid current leakage between the main power of the Carrier Board and the Suspend power of the Module, the SMBus on the Carrier Board must be separated by a bus switch from the SMBus of the Module. However, if the Carrier Board also uses Suspend powered SMBus devices that are designed to operate during system states S3-S5, then these devices must be connected to the Suspend powered side of the SMBus, i. e. between the COM Express Module and the bus switch. Since the SMBus is used by the Module and Carrier, care must be taken to ensure that Carrier based devices do not overlap the address space of Module based devices. Typical Module located SMBus devices and their addresses include memory SPD (serial presence detect 1010 000x, 1010 001x), programmable clock synthesizes (1101 001x), clock buffers (1101 110x), thermal sensors (1001 000x), and management controllers (vendor defined address). Contact Advantech for information on the SMBus addresses used.

2.13.1 SMB Signal Definitions

Table 37: SMB Signal Definitions

Signal	Pin#	Description	I/O	Pwr Rail	Note
SMB_CK	B13	System Management Bus bidirectional clock line Carrier Board: 3.3VSB SMBus device - Connect to SMBCLK of SMBus device. 3.3V SMBus device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SMBCLK of SMBus device. 5VSB SMBus device - Connect 5V Level Shifter to SMBCLK of SMBus device. 5V SMBus device - Connect 5V isolation circuit controlled by COME pin B24 PWR_OK to SMBCLK of SMBus device N/C if not used.	I/O OD CMOS	3.3V Suspend / 3.3V	
SMB_DAT	B14	System Management bidirectional data line. Carrier Board: 3.3VSB SMBus device - Connect to SMBDAT of SMBus device. 3.3V SMBus device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SMBDAT of SMBus device. 5VSB SMBus device - Connect 5V Level Shifter to SMBDAT of SMBus device. 5V SMBus device - Connect 5V isolation circuit controlled by COME pin B24 PWR_OK to SMBDAT of SMBus device N/C if not used.	I/O OD CMOS	3.3V Suspend / 3.3V	
SMB_ALERT#	B15	System Management Bus Alert Carrier Board: Connect to SMBALERT# of SMBus device. N/C if not used.	I CMOS	3.3V Suspend / 3.3V	

Note:

2.13.2 SMB Routing Guidelines

The SMBus should be connected to all or none of the PCIe devices and slots. A general recommendation is to not connect these devices to the SMBus.

The maximum load of SMBus lines is limited to 3 external devices. Please contact Advantech if more devices are required.

Contact Advantech for a list of SMBus addresses used on the Module. Do not use the same address for Carrier located devices.

2.13.3 SMB Trace Length Guidelines

Figure 32: Topology for SMB

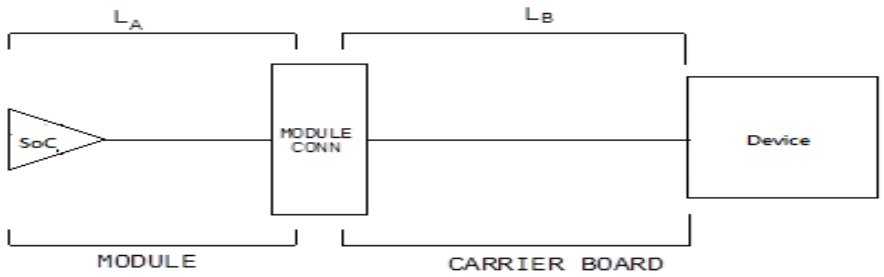


Table 38: SMB Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SMB	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 10mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	24”	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.14. General Purpose Serial Interface

Two TTL compatible two wire asynchronous serial ports are available on Module Types 7. This feature is introduced in COM.0 Revision 2 and uses pins on the A-B connector that have been re-claimed from the A-B VCC_12V pool.

Any of the Module asynchronous serial ports, if implemented on an Intel X86 architecture Module platform, ***should*** be I/O mapped serial ports that are register compatible with the National Semiconductor 16550 UARTs that were used in the PC AT architecture. The Module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the "console redirect" features available in many operating systems. The Module asynchronous serial ports ***should not*** be implemented as USB peripherals, as such implementations are generally not useful for low level debug purposes.

2.14.1 Serial interface Signal Definitions

Table 39: Serial interface Signal Definitions

Signal	Pin#	Description	I/O	Note
SER0_TX	A98	Transmit Line for Serial Port 0 Carrier Board: connect to Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS	
SER0_RX	A99	Receive Line for Serial Port 0 Carrier Board: Connect to Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS	
SER1_TX / CAN_TX	A101	Transmit Line for Serial Port 1 Carrier Board: connect to Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS	
SER1_RX / CAN_RX	A102	Receive Line for Serial Port 1 Carrier Board: Connect to Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS	

Note:

2.14.2 Serial interface Routing Guidelines

NA

2.14.3 Serial interface Trace Length Guidelines

Figure 33: Topology for Serial interface

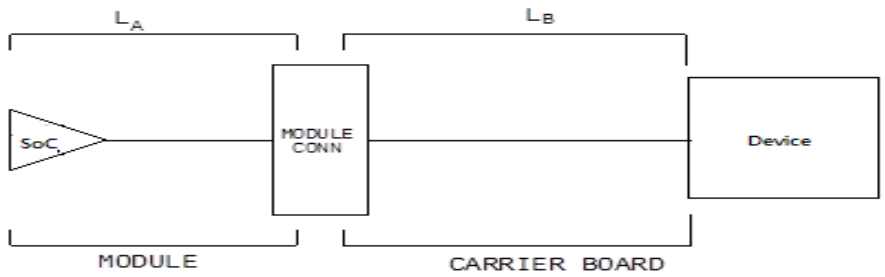


Table 40: Serial interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Serial interface	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-5992 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.15 CAN Interface *SOM-5992 is not support CAN Interface.

CAN Bus Operation Over SER1 Lines
The SER1_TX and SER1_RX asynchronous serial port lines defined for COM.0 Types 7 ***may*** be used alternatively to carry CMOS 3.3V logic level CAN (Controller Area Network) bus signals from a COM Express Module based CAN protocol controller. The CAN bus is an asynchronous, message based protocol widely used in the automotive and industrial control sectors. It is defined by ISO 11519, ISO 11898, and SAEJ2411. Data rates on a CAN bus ***may*** be as high as 1 MBit/s, although lower rates in the range from 10 kBit/s to 125 kBit/s are more common.
Use of the CAN bus in a COM Express system requires a CAN bus transceiver on the Carrier Board to interface to the CAN physical layer. CAN bus transceivers are available from NXP, Texas Instruments, Linear Technology, and others.
Data from the COM Express Module based CAN controller to the Carrier Board CAN transceiver is carried on Module line SER1_TX. Data from the Carrier Board CAN transceiver to the COM Express Module based CAN controller is carried on Module line SER1_RX. The Carrier Board CAN transceiver converts the logic level CAN protocol TX and RX signals from the Module into a differential half duplex line per the CAN specification.
How the SER1 asynchronous lines are shared with CAN bus operation is Advantech specific. Advantech ***may*** choose to use the SER1 TX and RX lines to support asynchronous serial port operation, or CAN bus operation, or both, or neither. Module build option(s) or software controlled muxing implementations ***may*** be used. **Please contact Advantech for information on the CAN Bus used.**

2.15.1 CAN interface Signal Definitions

Table 41: CAN interface Signal Definitions

Signal	Pin#	Description	I/O	Note
CAN_TX / SER1_TX	A101	Transmit Line for CAN Carrier Board: Check your CAN transceiver application notes.	O CMOS	1
CAN_RX SER1_RX	A102	Receive Line for CAN Carrier Board: Check your CAN transceiver application notes.	I CMOS	1

Note:

1. SOM-5992 is not support CAN Interface.

2.15.2 CAN interface Routing Guidelines

It should be routed as a differential pair signal with 120 Ohm differential impedance. The end points of CAN bus should be terminated with 120 Ohms or with 60 Ohms from the CAN_H line and 60 Ohms from the CAN_L line to the CAN Bus reference voltage. Check your CAN transceiver application notes for further details on termination.

2.15.3 CAN interface Trace Length Guidelines

Figure 34: Topology for CAN interface

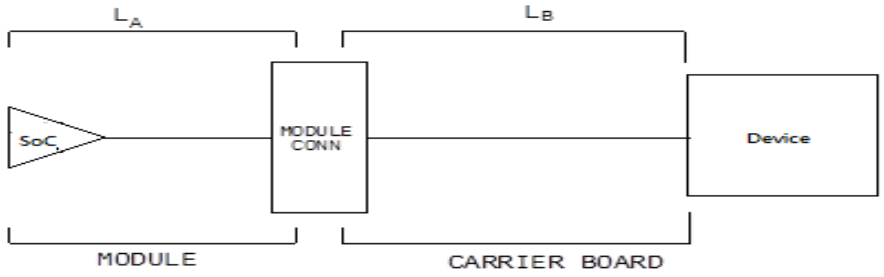


Table 42: CAN interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	CAN interface	1
Single End	NA	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	SOM-5992 is not support CAN Interface	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

1. SOM-5992 is not support CAN Interface

2.16 Miscellaneous Signals

2.16.1 Miscellaneous Signals

Table 43: Miscellaneous Signal Definitions

Signal	Pin#	Description	I/O	Note
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The Type pins indicate the COM Express pin-out type of the Module. To indicate the Module's pin-out type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pin-out type is detected.	O 5V PDS	Only Available on T2-T6 1. TYPE0# is GND pin. 2. TYPE1 is NC pin. 3. TYPE2# is GND pin.
TYPE10#	A97	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 2/Rev 3 Module is installed. TYPE10# NC Pin-out R3.x PD Pin-out Type 10 pull down to ground with 47k		1. TYPE10 is NC pin.
SPKR	B32	Output used to control an external FET or a logic gate to drive an external PC speaker. Carrier Board: Connect to Speaker circuit. N/C if not used	O 3.3V CMOS	
WDT	B27	Output indicating that a watchdog time-out event has occurred. Carrier Board: Connect to Watchdog trigger input. N/C if not used	O 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
LID#	A103	LID switch. Low active signal used by the ACPI operating system for a LID switch. Carrier Board: R2/R3 Module only - Connect to LID button. N/C if not used.	I 3.3V CMOS OD	
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. Carrier Board: R2/R3 Module only - Connect to Sleep button. N/C if not used	I 3.3V CMOS OD	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. Carrier Board: R2/R3 Module only - PD 4.7KΩ to GND and connects to FAN connector pin 2 PWMOUT via Smart FAN circuit N/C if not used	O 3.3V CMOS OD	
FAN_TACHIN	B102	Fan tachometer input for a fan with a two pulse output. Carrier Board: R2/R3 Module only - Connect to FAN connector pin 3 TACHIN via Smart FAN circuit N/C if not used	I 3.3V CMOS OD	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. Carrier Board: Physical Absence - N/C Physical Presence - PU 1KΩ to 3.3V N/C if not used	I 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
GPO0 / SDIO_CLK GPO1 / SDIO_CMD GPO2 / SDIO_WP GPO3 / SDIO_CD#	A93 B54 B57 B63	General Purpose Outputs for system specific usage. Carrier Board: Connect to GPO[3..0] N/C if not used	O 3.3V CMOS	1
GPI0 / SDIO_DAT0 GPI1 / SDIO_DAT1 GPI2 / SDIO_DAT2 GPI3 / SDIO_DAT3	A54 A63 A67 A85	General Purpose Input for system specific usage. The signals are pulled up by the Module. Carrier Board: Connect to GPI[3..0] N/C if not used	I 3.3V CMOS	1
VCC_RTC	A47	Real-time clock circuit power input. Nominally +3.0V		

Note:

1. SOM-5992 doesn’t support SDIO.

Table 44: Signal Definition SDIO

Signal	Pin#	Description	I/O	Notes
SDIO_CD# / GPO3	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Carrier Board: Connect to CD# of SDIO/MMC device or card N/C if not used	I 3.3V CMOS	1
SDIO_CLK / GPO0	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz Carrier Board: Connect to CLK of SDIO/MMC device or card N/C if not used	O 3.3V CMOS	1
SDIO_CMD / GPO1	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Carrier Board: Connect to CMD of SDIO/MMC device or card N/C if not used	O 3.3V CMOS	1
SDIO_WP / GPO2	B57	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Carrier Board: Connect to WP of SDIO/MMC device or card N/C if not used	I 3.3V CMOS	1
SDIO_DAT0 / GPI0 SDIO_DAT1 / GPI1 SDIO_DAT1 / GPI2 SDIO_DAT1 / GPI3	A54 A63 A67 A85	SDIO Data lines. These signals operate in push-pull mode. Carrier Board: Connect to DATA0-3 of SDIO/MMC device or card N/C if not used	I/O 3.3V CMOS	1

Note:

1. SOM-5992 doesn't support SDIO.

2.16.2 Power Management Signals

Signals PWR_OK, SYS_RESET#, and CB_RESET# ***shall*** be supported for all Module pinout types. Additionally, signal PWR_OK indicates that all the power supplies to the Module are stable within specified ranges and can be used to enable Module internal power supplies.
PWR_OK has been traditionally used to hold off a Module startup to allow devices on the Carrier such as FPGAs to initialize. The Module will typically not power up until the PWR_OK signal goes active. There is the potential for the Carrier to back drive voltages from the Carrier to the Module when the Carrier is powered but the Module is not.
The use of SYS_RESET# to hold off a Module startup may not produce the desired results since the behavior of SYS_RESET# is Module chipset dependent. In typical designs, the reset initiation happens on the falling edge of SYS_RESET# therefore holding the SYS_RESET# low will not result in preventing the Module for starting. PWR_OK ***should not*** be deactivated after the Module enters S0 unless there is a power fail condition.
Signals SUS_S3#, SUS_S4# and SUS_S5# define the signaling to indicate that the Module has entered the ACPI power-saving mode S3 (Suspend-To-RAM or STR), S4 (Suspend-To- Disk or STD), or S5 (Soft-Off).

Table 45: Power Management Signal Definitions

Signal	Pin#	Description	I/O	Note
PWRBTN#	B12	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge. Carrier Board: ATX - Connect to Power Button or SIO Power Button output pin (Active low) AT - N/C N/C if not used	I 3.3V Suspend CMOS	
SYS_RESET#	B49	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Carrier Board: Connect to Reset button N/C if not used	I 3.3V Suspend CMOS	
CB_RESET#	B50	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board. Carrier Board: Connect to reset pin of devices except PCIe slots or devices. N/C if not used.	O 3.3V Suspend CMOS	

Signal	Pin#	Description	I/O	Note
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Carrier Board: Connect to power good pin of main power supply ATX - PW-OK pin 8 of ATX power connector connects 3.3V level shifter to COME PWR_OK. AT - PG pin P8.1 of AT power connector connects 3.3V level shifter to COME PWR_OK. Other - PWROK of 12V power generator circuit connects 3.3V level shifter to COME PWR_OK. N/C is not allowed, if the system is ATX mode. N/C if not used.	I 3.3V CMOS	
SUS_STAT# /ESPI_RESET#	B18	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations. Carrier Board: Connect to LPCPD# of LPC device. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board *may* be used to enable the non-standby power on a typical ATX supply. Carrier Board: Connect to SLP_S3# (Suspend To RAM) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S4#	A18	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk). Carrier Board: Connect to SLP_S4# (Suspend To Disk) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S5#	A24	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off). Carrier Board: Connect to SLP_S5# (Soft Off) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	1

WAKE0#	B66	PCI Express wake up event signal. Module has integrated PU resistor to 3.3VDUAL Device - Connect to WAKE# pin of PCIE device. Slot - Connect to WAKE# pin B11 of PCIE slot. N/C if not used.	I 3.3V Suspend CMOS	
WAKE1#	B67	General purpose wake-up signal. Carrier Board: Connect to PME# of SIO N/C if not use	I 3.3V Suspend CMOS	
BATLOW#	A27	In a type 7 system, BATLOW# can be used as a power fail indication. Carrier Board: Connect to BATLOW# of Smart Battery. N/C if not used.	I 3.3V Suspend CMOS	

Note:

1. Connector to SUS_S4#.

2.16.3 Rapid Shutdown * SOM-5992 is not support.

COM Express Modules ***may*** support rapid shutdown. On a Module equipped with rapid shutdown, the assertion of the RAPID_SHUTDOWN input will cause the internal power supply regulators on the Module to be disabled, and for all residual voltages on the internal power supply rails to be discharged through crowbar circuits.

Modules supporting rapid shutdown ***shall*** specify the power rail discharge behavior, including discharge time constants and end-of-discharge voltages. An example of such a specification is “all internal power supply rails must decay to 37% of initial value within 300uS of RAPID_SHUTDOWN assertion, and to a voltage below 1.5V within 2mS of RAPID_SHUTDOWN assertion.”
A rapid shutdown implementation also requires supporting circuitry on the Carrier Board. Upon the assertion of RAPID_SHUTDOWN, the 12V (main) input power to the Module ***shall*** be removed by Carrier board circuitry and the input power pins ***shall*** be externally clamped to ground though a crowbar circuit located on the Carrier Board. This clamping circuit ***shall*** maintain a maximum resistance of 1 ohm and ***shall*** be active for a minimum of 2mS following the rise of RAPID_SHUTDOWN. The Module ***shall*** be designed with sufficiently low input capacitance to allow the input discharge specification to be met with a 1 ohm discharge resistance.
The Module design ***should*** prevent overheating or damage to any Module circuitry in the event that RAPID_SHUTDOWN is asserted without the removal of input power. This condition could occur due to malfunction of the Carrier Board support circuitry, or if the RAPID_SHUTDOWN signal is inadvertently asserted when the Module is installed on a Carrier Board that does not implement rapid shutdown support circuitry.
In some system implementations the power for both the Module and Carrier Board will fail shortly after the RAPID_SHUTDOWN signal is asserted. Therefore, the driving source for the RAPID_SHUTDOWN pin typically must charge an RC circuit on the Module that maintains crowbar assertion for several milliseconds following power failure. In order to charge this RC circuit rapidly, the RAPID_SHUTDOWN signal ***shall*** be sourced from a source impedance of 50 ohms or less. The RAPID_SHUTDOWN signal also ***shall*** have a rise time of <=1us and ***shall*** have a duration of >=20 uS. If the same RAPID_SHUTDOWN signal source is used to drive the Carrier Board input clamp circuitry, then any additional load from that Carrier Board circuitry needs to be considered in its design.

Table 46: Thermal Management Signal Definitions

Signal	Pin#	Description	I/O	Note
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Carrier Board: N/C if not used.	I 3.3V CMOS 5.0V Suspend/5.0V	1

Note:

1. SOM-5992 is not support.

2.16.4 Thermal Interface

Table 47: Thermal Management Signal Definitions

Signal	Pin#	Description	I/O	Note
THRM#	B35	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. Carrier Board: Connect to THRM# output of Hardware Monitor. N/C if not used.	I 3.3V CMOS	
THRMTRIP#	A35	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off). Carrier Board: Connect to THERMTRIP# input of devices. N/C if not used.	O 3.3V CMOS	

Note:

2.16.5 Miscellaneous Signals Routing Guidelines

NA

2.16.6 SDIO Signals Trace Length Guidelines

Figure 35: Topology for SDIO

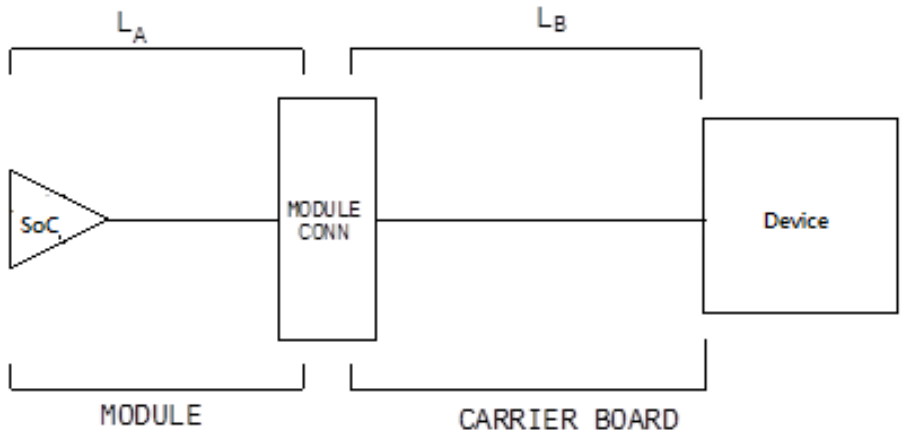


Table 48: SDIO Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SDIO	1
Single End	50Ω ±10%	1
DATA to CLK Maximum Pin to Pin Length Mismatch	500 mils	1
Main Route segment for CMD/Data/CD#	Minimum Trace Spacing Between Other SD Card and Interface Signals 5 mils	1
Main Route segment for CLK)	Minimum Trace Spacing Between Other SD Card and Interface Signals 15mils	1
Spacing to Other Signal Group	Min. 15mils	1
LA	SOM-5992 doesn't support SDIO.	1
LB	Carrier Board Length	1
Max length of LA+LB	"	1
Length matching	Data/CMD to Clock must be matched within 200mils	1
Reference Plane	Continuous ground only	1
Via Usage	Max 2 vias	1

Notes:

1. SOM-5992 don't support SDIO.

2.17 Reserved Pins.

RSVD pins are reserved for future use and should be no connect. But Advantech maybe use for another function, please see the 2.17.1 description.

2.17.1. Reserved Pins Definitions

Table 49: RSVD Definitions

Signal	Pin#	Description	I/O	Note
RSVD	A29	Reserved pin.		
RSVD	A30	Reserved pin.		
RSVD	A32	Reserved pin.		
RSVD	A33	Reserved pin.		
RSVD	A48	Reserved pin.		
RSVD	A86	Reserved pin.		
RSVD	A87	Reserved pin.		
RSVD	B28	Reserved pin.		
RSVD	B29	Reserved pin.		
RSVD	B30	Reserved pin.		
RSVD	C63	Reserved pin.		
RSVD	C64	Reserved pin.		
RSVD	C77	Reserved pin.		
RSVD	C83	Reserved pin.		
RSVD	C97	Reserved pin.		
RSVD	D36	Reserved pin.		
RSVD	D37	Reserved pin.		
RSVD	D54	Reserved pin.		
RSVD	D63	Reserved pin.		
RSVD	D64	Reserved pin.		
RSVD	D77	Reserved pin.		
RSVD	D83	Reserved pin.		
RSVD	D97	Reserved pin.		

Note:

3. Power

3.1. General Power requirements

COM Express calls for the Module to be powered by a single 12V power rail, with a +/-5% tolerance. The Basic format Modules are specified in COM.0 Rev. 3.x to support a power input range of 8.55V to 20.0V. Advantech offer a wide range input even on Compact and Basic Modules. COM Express Modules may consume significant amounts of power – 25 to 116W is common, and higher levels are allowed by the standard. Close attention must be paid by the Carrier Board designer to ensure adequate power delivery. Details are given in the sections below.

If Suspend functions such as Suspend-to-RAM, Suspend-to-disk, wake on power button press, wake on USB activity, etc. are to be supported, then a 5V Suspend power source must also be provided to the Module. If Suspend functions are not used, the Module VCC_5V_SBY pins should be left open. On some Modules, there may be a slight power efficiency advantage to connecting the Module VCC_5V_SBY rail to VCC_5V rather than leaving the Module pin open.

Please contact Advantech for further details. Carrier Boards typically require other power rails such as 5V, 3.3V, 3.3V Suspend, etc. These may be derived on the Carrier Board from the 12V and 5V Suspend rails.

3.2. ATX and AT Power Sequencing Diagrams

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 35 below.

A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 36 below .

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details.

Figure 36: ATX Style Power Up Boot – Controlled by Power Button

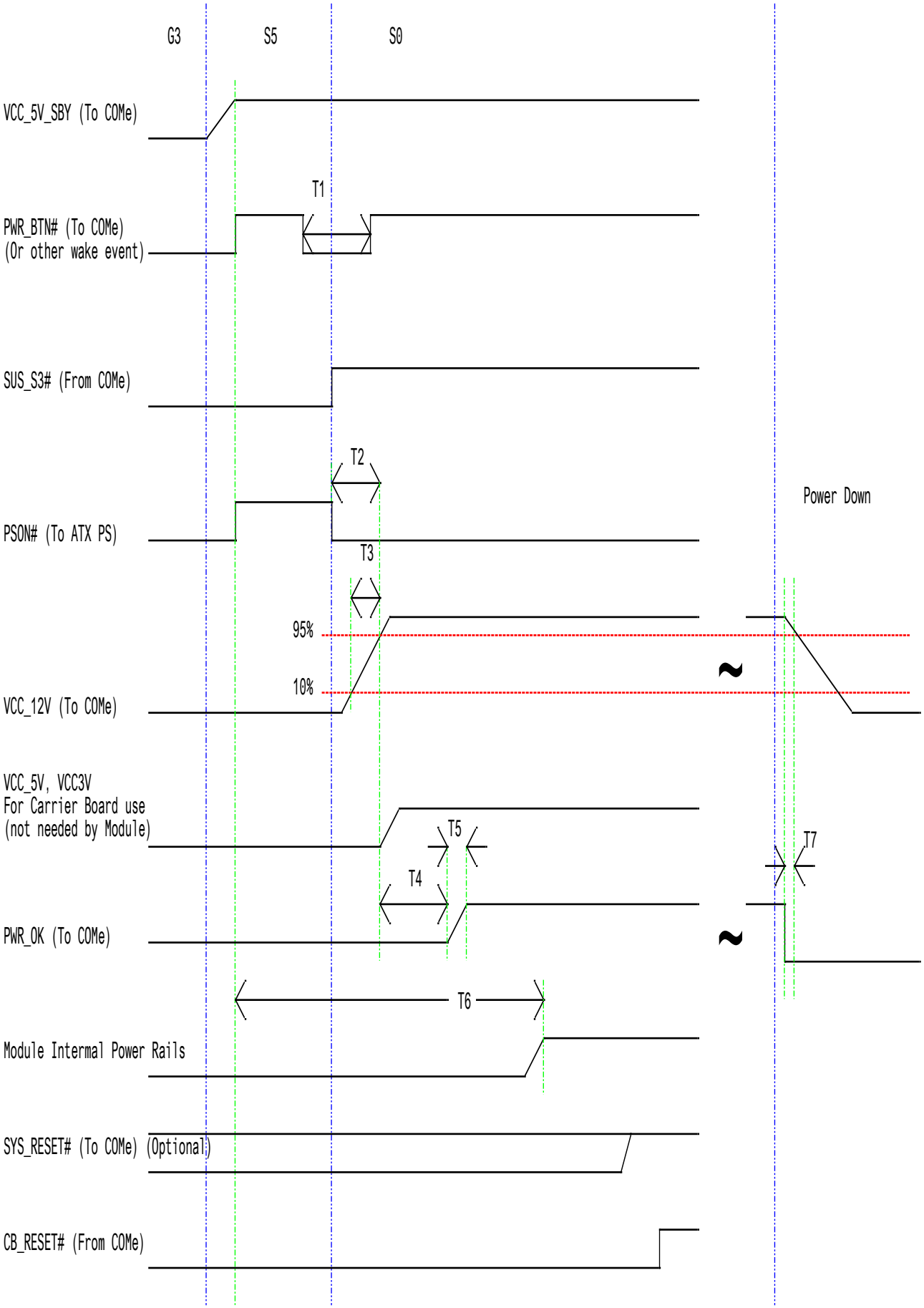


Figure 37: AT Style Power Up Boot

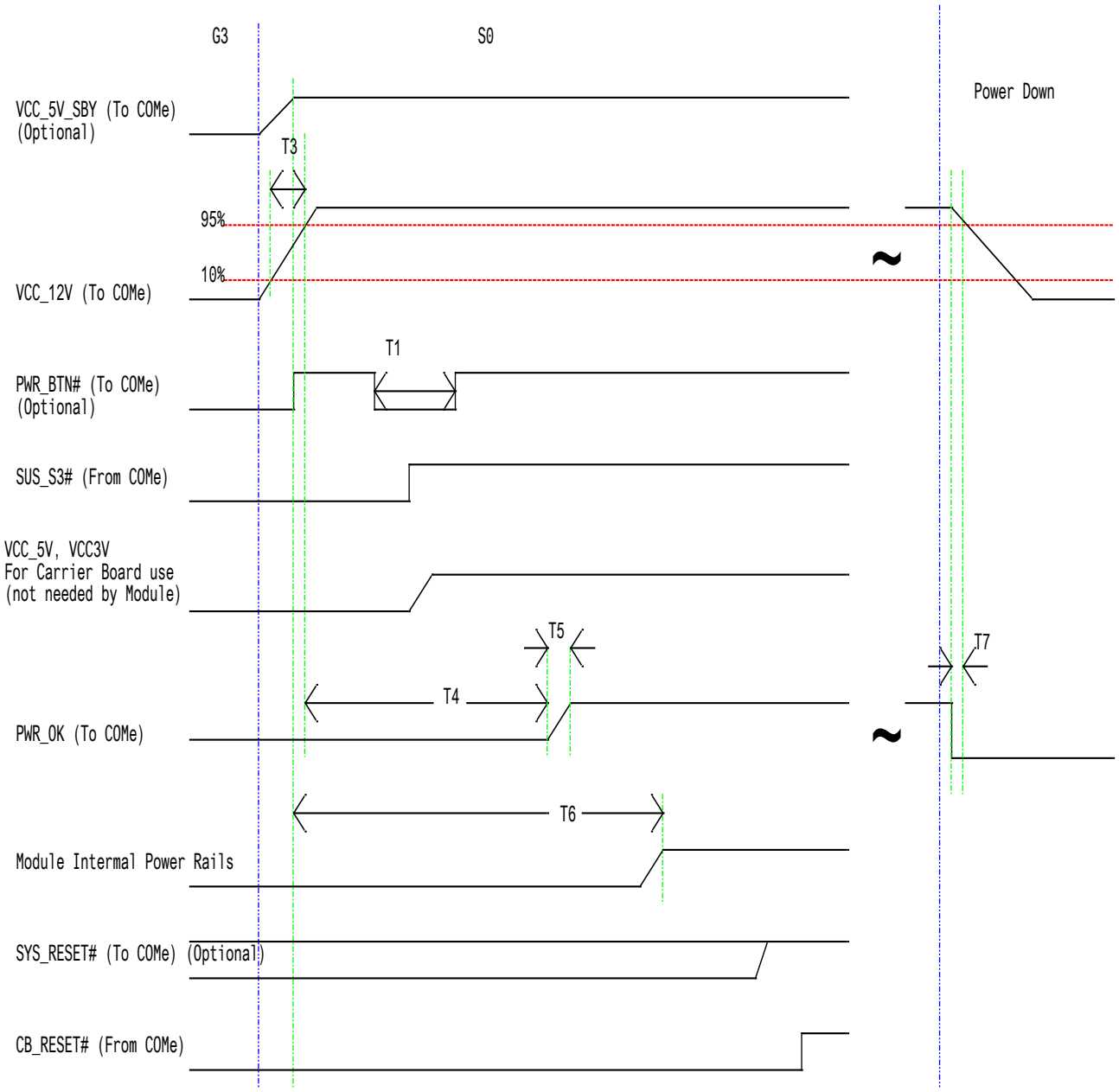


Table 50: Power Management Timings

Sym	Description	Min	Max
T1	Power Button	16ms	
T2	The power-on time is defined as the time from when PS_ON# is pulled low to when the VCC_12V, VCC_5V and VCC_3V output.		500ms
T3	VCC_12V rise time from 10% to 95%	0.1ms	20ms
T4	PWR_OK delay	100ms	
T5	PWR_OK rise time		10ms
T6	See Note 1		
T7	Power-down warning	1ms	

Note:

1. There is a period of time (T6 in Figure 35 and Figure 36 above) during which the Carrier Board circuits have power but the COM Express Module main internal power rails are not up. This is because almost all COM Express internal rails are derived from the external VCC_12V and there is a non-zero start-up time for the Module internal power supplies.

Carrier Board circuits should not drive any COM Express lines during the T6 interval except for those identified in the COM Express Specification as being powered from a Suspend power rail. Almost all such signals are active low. Such signals, if used, should be driven low by open drain Carrier Board circuits to assert them. Pull-ups, if present, should be high value (10K to 100K) and tied to VCC_5V_SBY.

The line PWR_OK may be used during the T6 interval to hold off a COM Express Module boot. Sometimes this is done, for example, to allow a Carrier Board device such as an FPGA to be configured before the Module boots.

The deployment of Carrier Board pull-ups on COM Express signals should be kept to a minimum in order to avoid back-driving the COM Express signal pins during this interval.
Carrier Board pull-ups on COM Express signal pins are generally not necessary – most signals are pulled up if necessary on the Module.

3.3. Design Considerations for Carrier Boards containing FPGAs/CPLDs

Very often, the Carrier Board will contain custom FPGA or other programmable devices which require the loading of program code before they are usable. The Carrier Board designer needs to take the necessary precautions to ensure that his Carrier Board logic is up and running before the Module starts. Conflicts can occur if the Module is powered on and allowed to run before devices on the Carrier Board are fully programmed and initialized. A typical example is an FPGA which includes a PCIe device. Such devices must be initialized and ready before the chipset on the Module performs link training and before the BIOS code performs enumeration of PCI devices. The Module should therefore be prevented from starting before Carrier Board devices are ready.

One method to achieve this is to delay assertion of the PWR_OK# signal to the Module until the Carrier Board initialization process has completed. Note that during the phase when the Carrier Board is powered and the Module is not powered there is potential for back drive voltages from the carrier to the Module.

Another possibility is to use the SYS_RESET# signal to delay Module start-up. However, depending on the Module implementation and the chipset used, SYS_RESET# may only be a falling edge triggered signal and not a low active signal as was originally intended. In that case, asserting SYS_RESET# may not hold the Module in the reset state. Also, PCIe link training will occur regardless of the reset signal state for some chipsets.

Please refer to the COM.0 R3.x specification (Power and System Management section) for more details and check the Module provider’s documentation for their implementations of these signals.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 51: Absolute Maximum Ratings

SOM-5992		MIN	MAX	UNIT
Power	VIN	8.5 (5-5%)	20(19+5%)	V
	VSB	4.75 (5-5%)	5.25 (5+5%)	V
	RTC Battery	2.0	3.3	V

4.2. DC Characteristics

Table 52: DC Current Characteristics1

Intel D-1548 @2.0GHz (PTU)				
Power Plane	Maximum Power Consumption			
Symbol	S0	S3	S5	G3
+VIN (+12V)	55.53W	--	--	--
+VIN (+8.5V)	52.82W	--	--	--
+VIN (+20V)	54.97W	--	--	--
+V5SB_CB	0.045W	--W	1.761W	--
RTC Battery	--	--	1.48uA	4.04uA

Table 53: DC Current Characteristics2

Intel D-1548 @2.0GHz (Burn-in)				
Power Plane	Maximum Power Consumption			
Symbol	S0	S3	S5	G3
+VIN (+12V)	50.26W	--	--	--
+VIN (+8.5V)	49.35W	--	--	--
+VIN (+20V)	51.52W	--	--	--
+V5SB_CB	0.03W	--W	1.761W	--
RTC Battery	--	--	1.48uA	4.04uA

4.3. Inrush Current

Table 54 : Inrush Current

Power Plane	Maximum	
Symbol	G3 to S5	S5 to S0
+V5SB_CB	1.2708A	-----
+VIN (+12V)	-----	2.54070A
+VIN (+8.5V)	-----	3.2156A
+VIN (+20V)	-----	1.7559A