PCLD-782B
24/16 Channel Opto-isolated D/I Board

USER'S MANUAL

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CHAPTER 1. INTRODUCTION

The PCLD-782B is a 24/16 channel digital input daughterboard, featuring high-voltage (>1500 V_{DC}) opto-isolation on all inputs. It can be used by all PC-LabCards with D/I channels on either 20-pin flat ribbon connectors, or 50-pin opto-22 connectors.

The PCLD-782B has on-board screw terminals for easy input wiring. The opto-isolated signal conditioning provides isolation between channels, and also between each input and the PC. This is the ideal solution for preventing floating potential and ground loop problems, while also giving protection from potentially damaging fault conditions on the input lines.

Each input channel is equipped with a red LED to indicate input status. If the input signal is high, the LED will be ON. Users may configure each channel to work in either isolated or non-isolated mode.

1.1. Applications

- Digital signal sensing
- Switch status monitoring
- Limit switch monitoring

1.2. Features

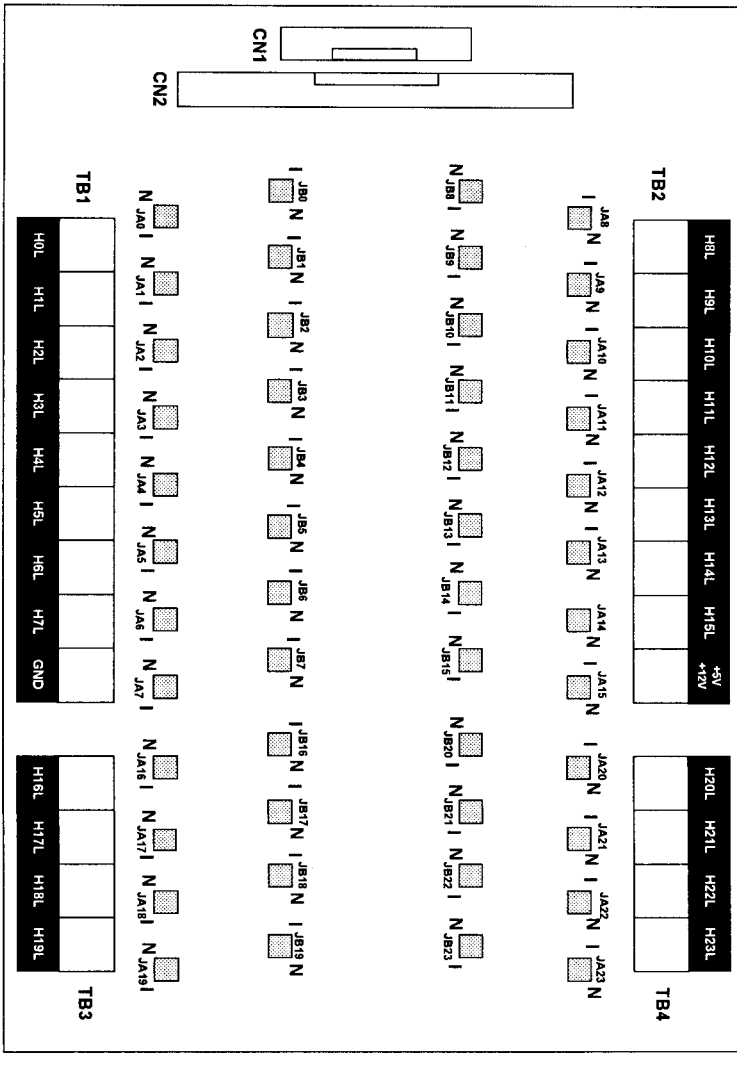
- Compatible with all PC-LabCards featuring D/I channels on either 20-pin flat cable or 50-pin opto-22 connectors
- 24 opto-isolated digital input channels
- On-board signal conditioning circuits
- Built-in screw terminals for easy input wiring
- LEDs indicate input logic status
- Inputs buffered with voltage comparators

1.3. Specifications

- **Input channels** : 24
- **Input range** : 0 ~ 24 V_{DC}
- **Input resistance** : 560 Ω
- **Isolation voltages** : >1500 V_{DC} channel to channel
  >1500 V_{DC} channel to PC
- **Threshold voltage** : 1.5 V_{DC} VR adjustable
- **Screw terminals** : Accept #22 to #12 AWG wires
- **Connector for digital bus** : 20-pin flat cable connector, or 50-pin opto-22 connector
- **Dimensions** : 220 mm (L) x 132 mm (W)

CHAPTER 2. CONFIGURE SETTING

2.1. PCLD-782B Board Layout



2.2. Output Connectors

The PCLD-782B has two output connectors, CN1 and CN2. CN1 is a 20-pin connector. The output signals on CN1 follow the input signals; that is, when the input signal is HIGH, then the output is TTL HIGH. CN2 is a 50-pin opto-22 connector. The output signals on CN2 are inverted from the input; that is, when the input signal is HIGH, then the output is TTL LOW.

The tables on the following pages show pin assignments for CN1 and CN2, terminal block (TB1 and TB2) terminal numbers, and the related LED and jumper groups for each of the 24/16 input channels.

Table 1 shows the 20-pin connector CN1 (16 channels), and Table 2 shows the 50-pin connector CN2 (24 channels).

Table 1 (CN1)

CN1 Pin Number	TB1 and TB2 Label Name	Related LED	Related Jumpers
1	TB1 0H, 0L	D0	JA0, JB0
2	TB1 1H, 1L	D1	JA1, JB1
3	TB1 2H, 2L	D2	JA2, JB2
4	TB1 3H, 3L	D3	JA3, JB3
5	TB1 4H, 4L	D4	JA4, JB4
6	TB1 5H, 5L	D5	JA5, JB5
7	TB1 6H, 6L	D6	JA6, JB6
8	TB1 7H, 7L	D7	JA7, JB7
9	TB2 8H, 8L	D8	JA8, JB8
10	TB2 9H, 9L	D9	JA9, JB9
11	TB2 10H, 10L	D10	JA10, JB10
12	TB2 11H, 11L	D11	JA11, JB11
13	TB2 12H, 12L	D12	JA12, JB12
14	TB2 13H, 13L	D13	JA13, JB13
15	TB2 14H, 14L	D14	JA14, JB14
16	TB2 15H, 15L	D15	JA15, JB15
17	GND		
18	GND		
19	+5 V		
20	+12 V		

Table 2 (CN2)

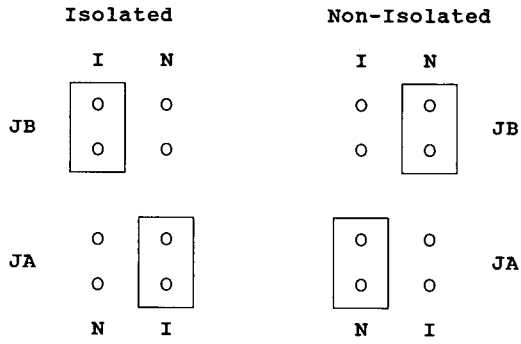
CN2 Pin Number	TB1,TB2, TB3 and TB4 Label name	Related LED	Related Jumpers
1	TB4 23H, 23L	D23	JA23, JB23
3	TB4 22H, 22L	D22	JA22, JB22
5	TB4 21H, 21L	D21	JA21, JB21
7	TB4 20H, 20L	D20	JA20, JB20
9	TB3 19H, 19L	D19	JA19, JB19
11	TB3 18H, 18L	D18	JA18, JB18
13	TB3 17H, 17L	D17	JA17, JB17
15	TB3 16H, 16L	D16	JA16, JB16
17	TB2 15H, 15L	D15	JA15, JB15
19	TB2 14H, 14L	D14	JA14, JB14
21	TB2 13H, 13L	D13	JA13, JB13
23	TB2 12H, 12L	D12	JA12, JB12
25	TB2 11H, 11L	D11	JA11, JB11
27	TB2 10H, 10L	D10	JA10, JB10
29	TB2 9H, 9L	D9	JA9, JB9
31	TB2 8H, 8L	D8	JA8, JB8
33	TB1 7H, 7L	D7	JA7, JB7
35	TB1 6H, 6L	D6	JA6, JB6
37	TB1 5H, 5L	D5	JA5, JB5
39	TB1 4H, 4L	D4	JA4, JB4
41	TB1 3H, 3L	D3	JA3, JB3
43	TB1 2H, 2L	D2	JA2, JB2
45	TB1 1H, 1L	D1	JA1, JB1
47	TB1 0H, 0L	D0	JA0, JB0
49	+5 V		
Even pins	GND		

2.3. Isolated or Non-isolated Input

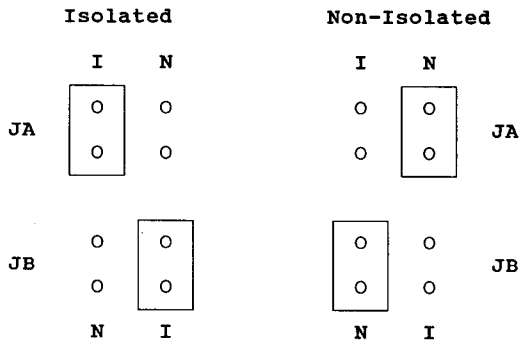
Each digital input channel on the PCLD-782B is equipped with a pair of jumpers to select the input mode as either isolated or non-isolated.

Examples for setting the input mode are shown below. Note that the isolated/non-isolated jumper settings for channels 0-7 and 16-19 are different from those of channels 8-15 and 20-23.

Channels 0 to 7, and Channels 16 to 19



Channels 8 to 15, and Channels 20 to 23



Note: The factory default setting is **Isolated Mode** for all channels

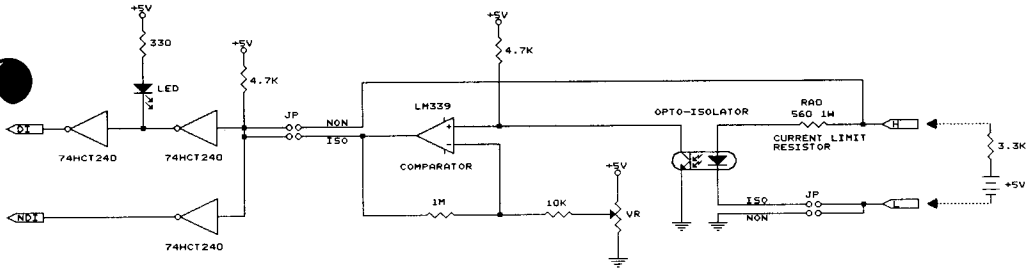
CHAPTER 3. CALIBRATION AND TEST

3.1. Threshold Adjustment for Isolated Input Mode

The PCLD-782B is equipped with a variable resistor (VR1) to adjust the threshold level for all 24 isolated input channels.

In the isolated input mode, the PCLD-782B is actually driven by input current, rather than input voltage. Sometimes, due to the input leakage current effect, the input status will be a constant logic high, although the input voltage level is low.

The circuit diagram shown below may be used to prevent input leakage current effect, and the following test procedure may be used to set the threshold level.



3.2. Test Procedure

1. Apply a 5 V_{DC} signal to input terminals 0L and 0H. Include a 3.3 KΩ resistor in series with the voltage source as shown in the diagram below. This circuit will supply about 1 mA to the opto-isolator.

2. Adjust VR1 until LED 0 turns off.

The above adjustment ensures that if channel 0's input voltage is low, and the input leakage current is less than 1 mA, the input status will be considered as logic low (TTL 0). The value of the series resistor shown as 3.3 KΩ in the diagram should be selected to meet local requirements.

3.3. Customizing the Current Limit Resistor

The default voltage input range of the PCLD-782B is from 0 to 24 V_{DC}. If it is desired to accept higher voltage inputs, users can replace the current limit resistors, RA0 through RA23, for each channel.

It is easy to choose the proper current limit resistor. Since the opto-isolator has a current rating of 60 mA, your input current must not exceed this value. The formula used to calculate the resistor value is shown below:

$$\mathbf{I_{in} = V_{in} / R_{limit}}$$

where I_{in} : input current (in A)
V_{in} : input voltage (in V)
R_{limit} : current limit resistor (in Ω)

Note: It is suggested that the value I_{in} should be held to 20 mA.

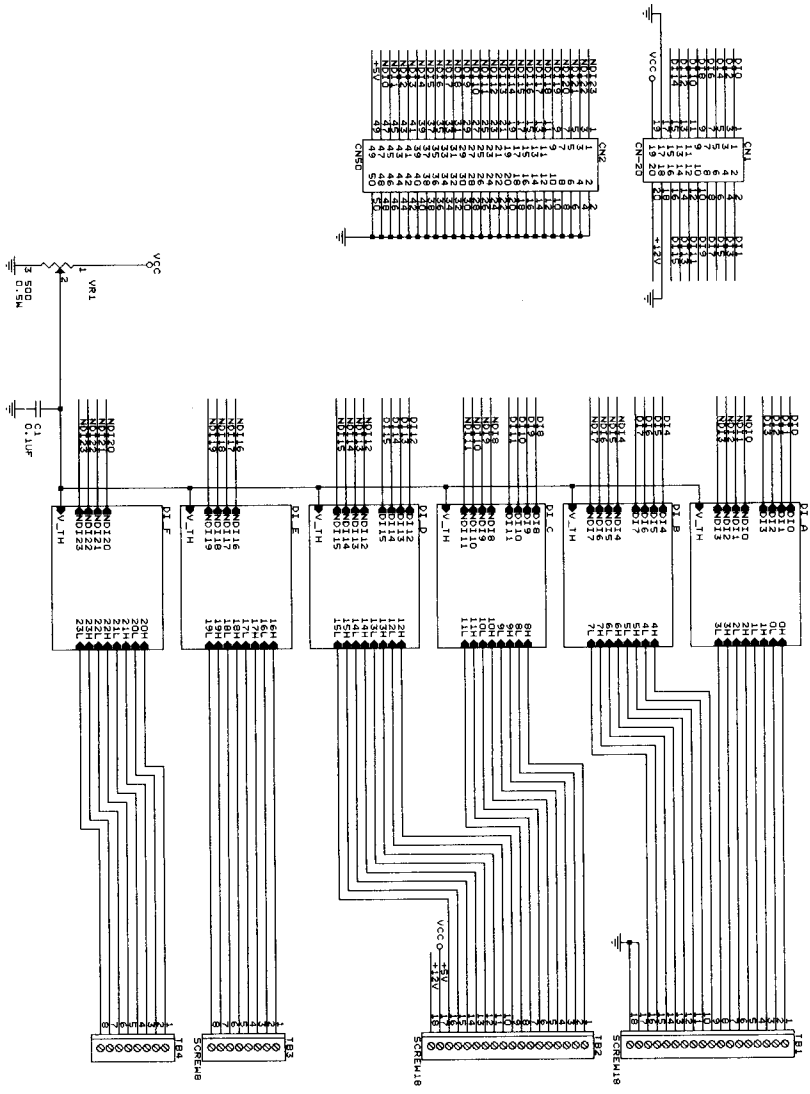
In addition, you should consider the current limit resistor's maximum power rating. The maximum power consumption should not exceed the power rating of your resistor. The appropriate formula is shown below:

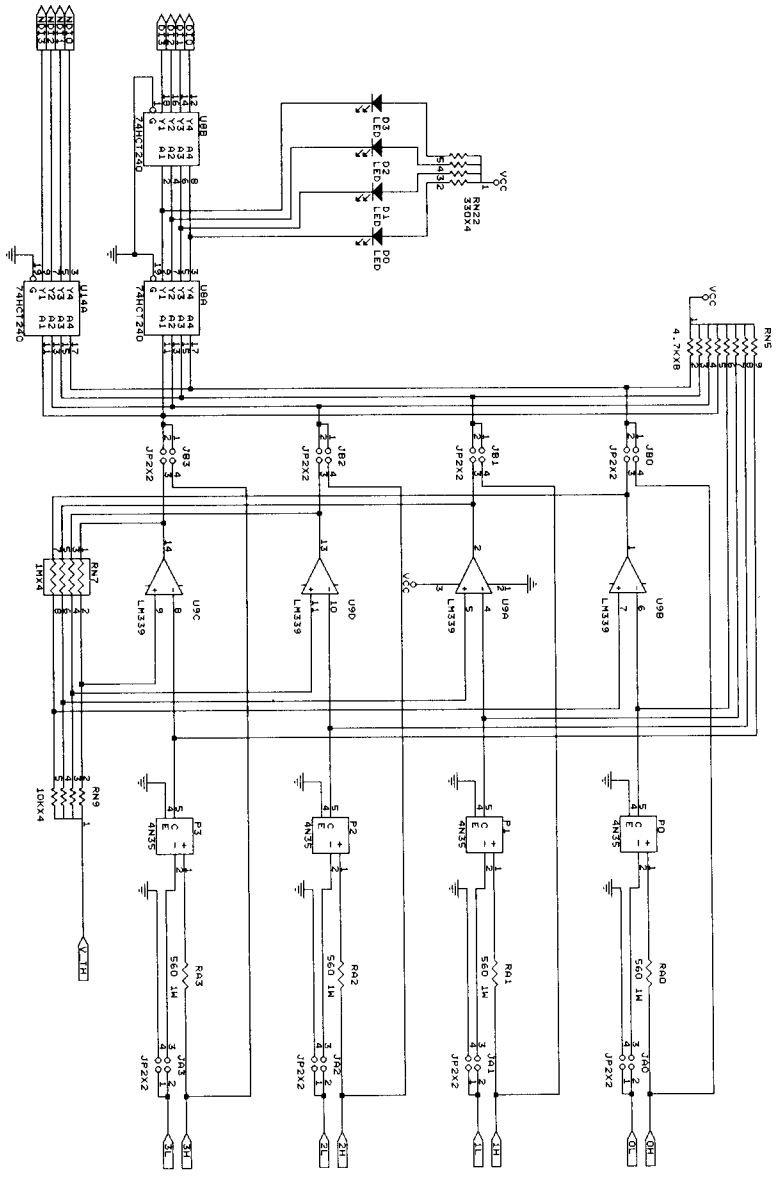
$$\mathbf{P_{in} = V_{in} * I_{in}}$$

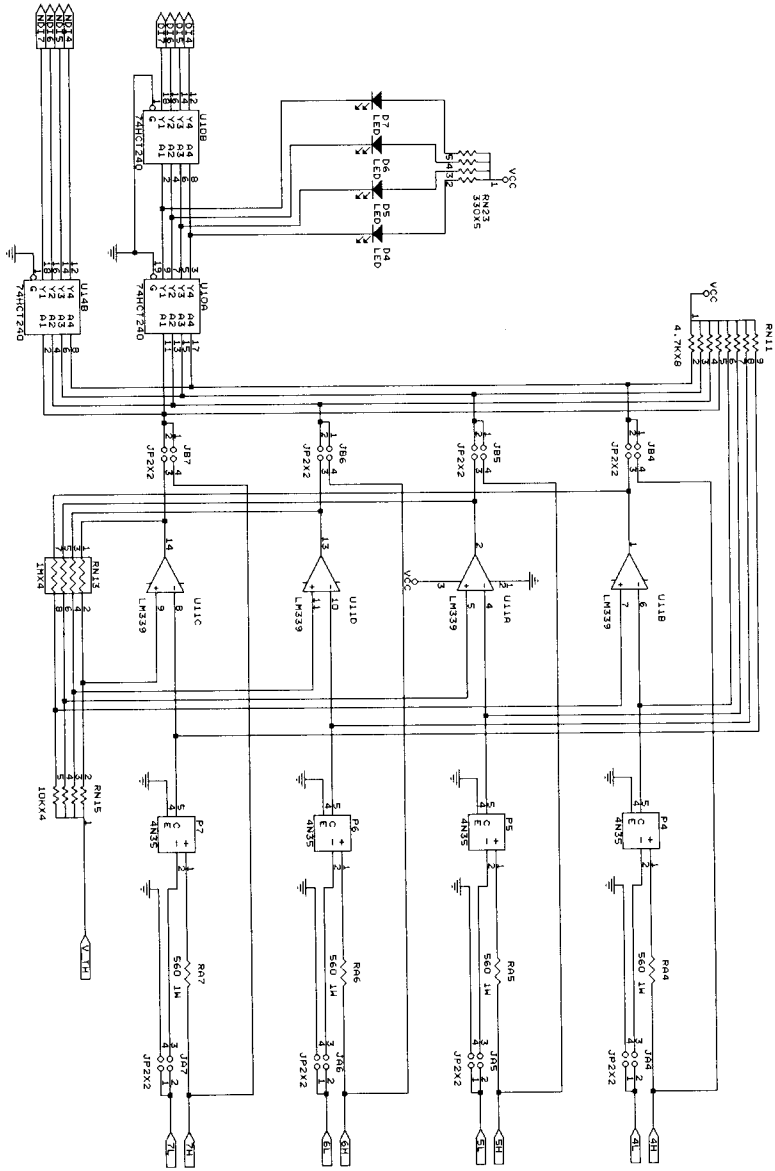
where I_{in} : input current (in A)
V_{in} : input voltage (in V)
R_{limit} : current limit resistor (in Ω)

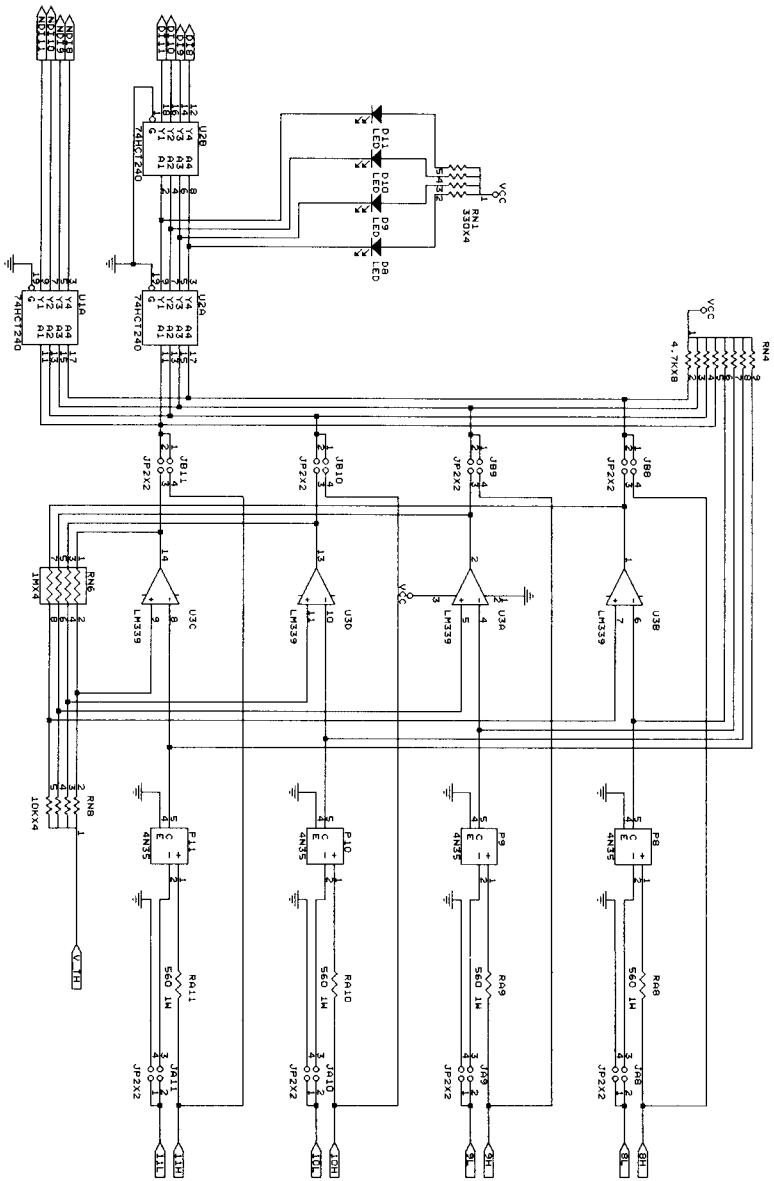
For example, if your maximum voltage input is 50 V, and the current limit resistor you have chosen is 1 KΩ, then the maximum input current will be 50 mA. The power consumption of the current limit resistor will be approximately 2.5 W. In such a situation, the power rating of your resistor should be at least 2.5 W.

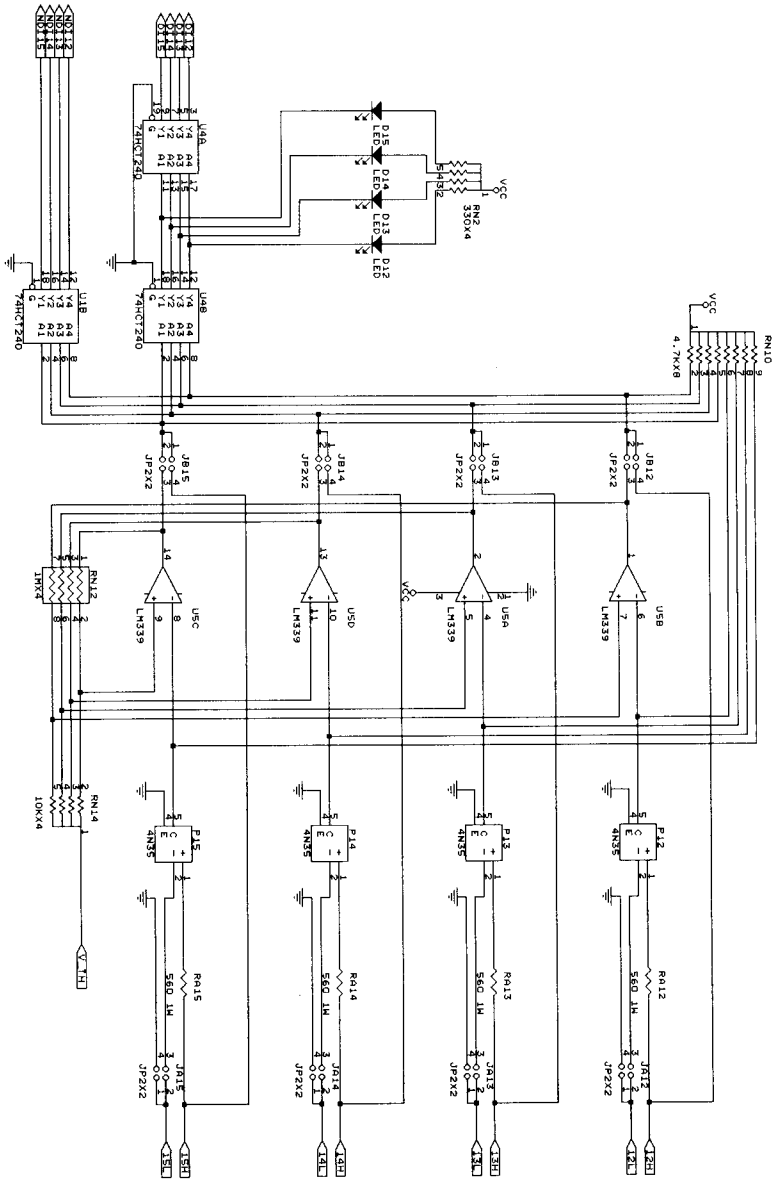
Appendix Circuit Diagram

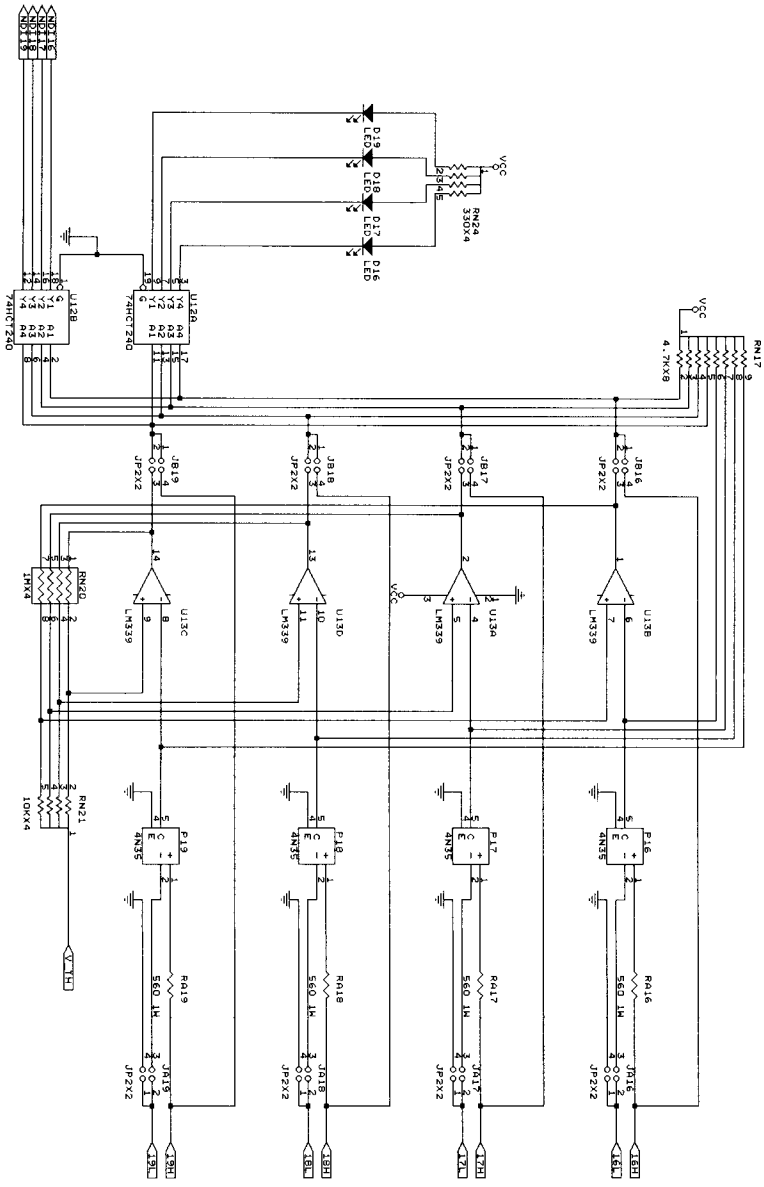











RN15
RN16
74HCT240
U12B
U12A
74HCT240
D19 LED
D18 LED
D17 LED
D16 LED
RN24 330X4
VCC
RN17 4.7KX8
JP2X2
JB19
JB18
JB17
JB16
RN20 1MX4
RN21 10KX4
LM339
U13C
U13D
U13A
U13B
2N35
P19
P18
P17
P16
RA19 560 1W
RA18 560 1W
RA17 560 1W
RA16 560 1W
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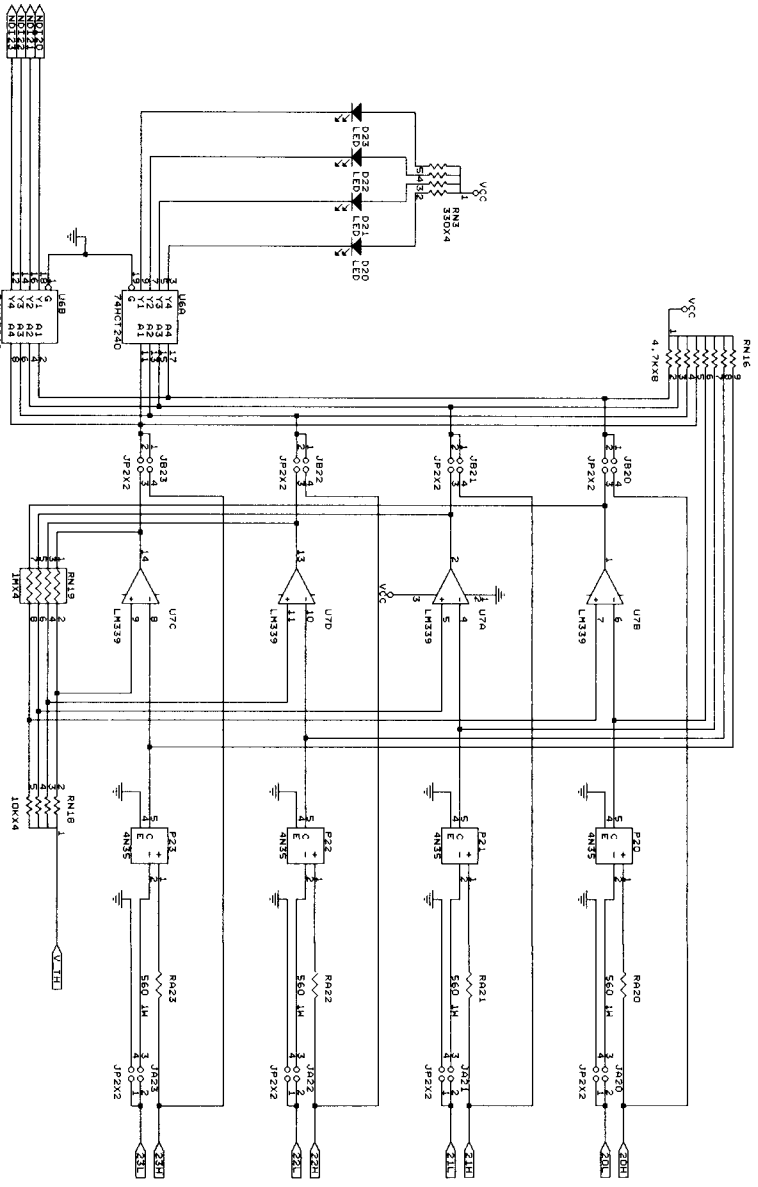
-18H
-17L
-17H
-16L
-16H
V_TH


NOT USED
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NOT USED
NOT USED
D23 LED
D22 LED
D21 LED
D20 LED
RN3 330X4
VCC
74HCT240
U6B
U6A
RN16 4.7KX8
JP2X2
JB23
JB22
JB21
JB20
RN19 1KX4
LM339
U7C
U7D
U7A
U7B
RN18 10KX4
4N35
P23
P22
P21
P20
R423
R422
R421
R420
560 1/4W
JA23
JA22
JA21
JA20
23L
23H
22L
22H
21L
21H
20L
20H
V_TH