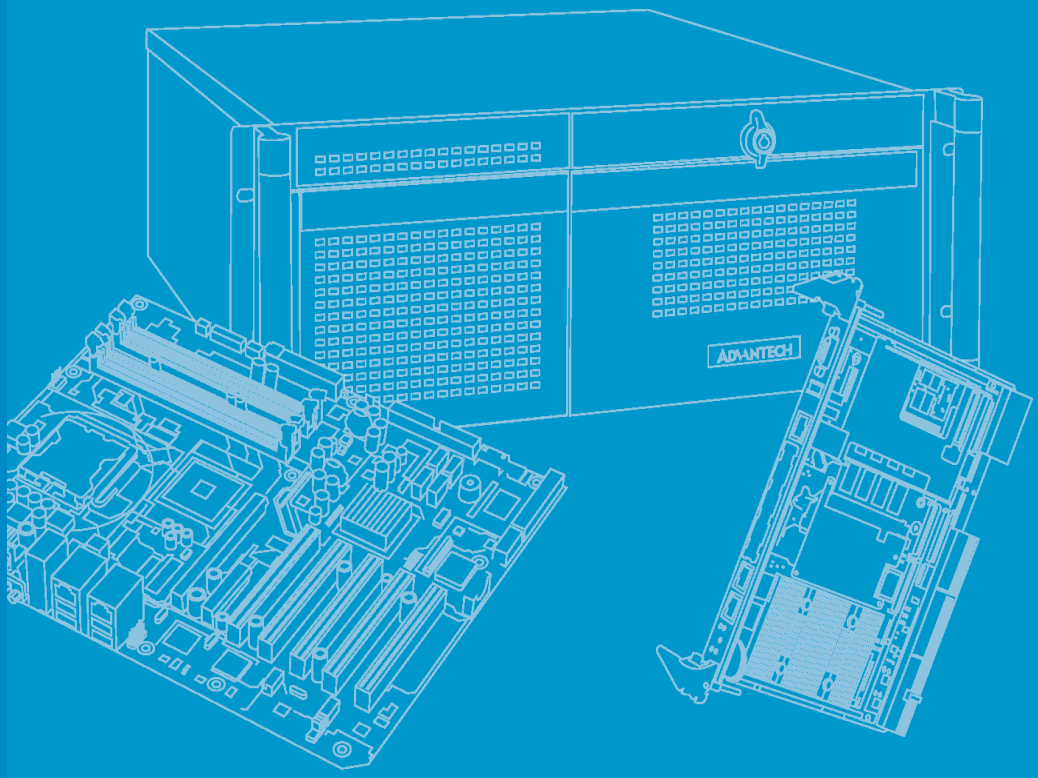


User Manual

MIC-3395

6U CompactPCI® 2nd Generation Intel® Core™ i3/i5/i7 Processor Blade with ECC support

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgements

Intel® and Pentium® are trademarks of Intel Corporation.

Microsoft® Windows® and MS-DOS® are registered trademarks of Microsoft Corp.

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Part No. 2002339501 Edition 2

Printed in Taiwan June 2012

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such, in writing, to:
support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- MIC-3395 all-in-one single board computer (CPU heatsink and PCH heatsink included) x1
- Daughter board for SATA HDD (Assembled) x1
- HDD tray and screws x 1
- Solder-side cover (Assembled) x1
- RJ45 to DB9 cable x1
- Warranty certificate document x1
- Safety Warnings: CE, FCC class A

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden electrostatic discharge as you connect a jumper or install a card can damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

Contents

Chapter 1

Hardware Configuration

This chapter describes how to configure MIC-3395 hardware.

1.1 Introduction

The MIC-3395 is a high performance, power efficient CompactPCI single-board computer based on the Intel® Core™ i3/i5/i7 microprocessors. The MIC-3395 delivers breakthrough energy-efficient performance for CompactPCI platforms. The Intel® Core™ i3/i5/i7 provides enhanced energy-efficient performance to help equipment manufacturers optimally balance processing capabilities within power and space constraints. The advanced smart cache of Core™ i3/i5/i7 dynamically allocates the shared L2 cache across cores and optimizes use of memory subsystem bandwidth to accelerate out-of-order execution. A prediction mechanism reduces the time in-flight instructions have to wait for data. The new pre-fetch algorithms move data from system memory into fast L2 cache in advance of execution.

The Core™ i3/i5/i7 combines the benefits of two high- performance execution cores with intelligent power management features to deliver significantly greater performance per watt over previous Intel processors. The two execution cores share a high-performance, power-optimized 5GT/s DMI bus to access the same system memory. To save power, address and data buffers are turned off when there is no activity.

The MIC-3395 maximizes I/O throughput with PCI Express (PCIe) technology. An onboard 4 GB of 1333 MHz DDR3 memory is provided with a combination of SO-DIMM up to 2 GB of 1333 MHz DDR3 as option. It supports a fast Serial-ATA interface to an on-board hard drive.

1.2 Specifications

1.2.1 CompactPCI Bus Interface

The MIC-3395 is compliant with PICMG 2.0 Rev. 3.0. It supports a 64-bit / 66 MHz or 33MHz PCI bus for up to 7 CompactPCI slots at 3.3 V or 5 V VIO. The MIC-3395 is hot-swap compliant (PICMG 2.1) and conforms to the CompactPCI Packet Switching Backplane specification (PICMG 2.16) as well as the CompactPCI System Management Specification (PICMG 2.9).

The board can be configured as a system master or a drone board. In drone mode it only draws power from the CompactPCI backplane and is not active on the CompactPCI bus. However, PICMG 2.16 is still fully supported in this mode.

1.2.2 CPU

The MIC-3395 supports Intel 2nd generation Core i3/i5/i7 Sandy Bridge processor family with clock frequencies up to 2.2 GHz and a Direct Media Interface (DMI) up to 5 GT/s.

Intel 2nd generation Core i3/i5/i7 processors are validated with Intel mobile QM67 chipset. This chipset provides greater flexibility by deploying the latest virtualization, multi-threading and I/OAT acceleration techniques, as well as remote asset management capabilities, and improved storage speed and reliability.

Supported processors are listed in the table below. The Intel 2nd generation Core i3/i5/i7 processor support up to two cores / four threads at 2.2 GHz and 4 MB L2 cache.

1.2.3 Processor

Table 1.1: Processor Type

Model Number	CPU architecture	# cores	Freq.	Cache	DMI	CPU TDP	Package	Required airflow
I7-2655LE	Sandy Bridge (32 nm)	2	2.2 GHz	4 MB	5 GT/s	25 W	FCBGA	30 CFM
I5-2515E	Sandy Bridge (32 nm)	2	2.5 GHz	3MB	5 GT/s	35W	FCBGA	30 CFM
I7-2715QE	Sandy Bridge (32nm)	4	2.1 GHz	6MB	5 GT/s	45W	FCBGA	35 CFM

Note! *Because power consumption and thermal restrictions vary between different CompactPCI systems, please double check these items before installing a higher speed CPU not listed in the table above.*

1.2.4 BIOS

An 8 Mbyte SPI flash contain a board-specific BIOS (from AMI) designed to meet industrial and embedded system requirements.

1.2.5 Chipset

The Intel Mobile QM67 chipset provides excellent flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth over previous Intel chipsets, as well as remote asset management capabilities and improved storage speed and reliability.

The Mobile Intel QM67 chipset offers up to 5 GT/s for fast access to peripheral devices.

It delivers outstanding system performance through high bandwidth interfaces such as PCI Express, Serial ATA and Hi-Speed USB 2.0.

1.2.6 Memory

The MIC-3395 has up to 4 GB of onboard with ECC support DDR3 memory. It also has one 240-pin SO-DIMM sockets that can accommodate an additional 2GB of memory. The following table shows a list of SO-DIMM modules that have been tested on the MIC-3395.

Table 1.2: Memory Type

Brand	Size	Speed	Vendor PN	ECC	Pin Count	Memory Chip
ATP	2 GB	DDR3 1333	AW56M7228BJH9S	Yes	204 - pin	Samsung 128MX8X18 30mm, 2-Rank
	4 GB	DDR3 1333	AW12M7228BKH9S	Yes	204 - pin	Samsung 256MX8X18 30mm, 2-Rank
SMART	2 GB	DDR3 1333	SG572568FH8DZPH1	Yes	204 - pin	Samsung 128MX8X18 30mm, 2-Rank
	4 GB	DDR3 1333	SG572128FH8DZPH	Yes	204 - pin	Samsung 256MX8X18 30mm, 2-Rank
Transcend	4 GB	DDR3 1333	TS7KPN20100-3Y	Yes	204 - pin	Hynix 256MX8X18 30mm, 2-Rank

Table 1.2: Memory Type						
Memphis	2 GB	DDR3 1333	SODD3256M723G-D28MTD	Yes	204 - pin	Micron 256MX8X9 30mm, 1-Rank
	4 GB	DDR3 1333	SODD3512M723G-C28MTD	Yes	204 - pin	Micron 256MX8X18 30mm, 2-Rank

Note! *8 GB on board memory is optional. Please inform you local sales.*

1.2.7 Ethernet

The MIC-3395 uses one Intel® 82574L and one Intel® 2579LM LAN chips to provide 10/100/1000 Mbps Ethernet connectivity (LAN1 & LAN2) and four Intel 82574L LAN chips to provide 10/100/1000 Mbps Ethernet connectivity (LAN3~LAN6) via rear I/O. Optional settings for the source of each individual Gigabit Ethernet port can be selected in the BIOS menu. These are mutually exclusive and can be any one of:

- Front I/O (RJ-45)
- Rear I/O (Rear Transition Module)
- PICMG 2.16

1.2.8 Storage Interface

The MIC-3395 supports one SATA III and three SATA II interfaces. The SATA III interface can be routed to an onboard 2.5" SATA hard disk drive or to the rear I/O module via the J5 connector. The SATA II interface is connected to the rear I/O module via the J5 connector and is reserved for user customized designs. Currently, Advantech's compatible RIO modules provide the SATA II.

1.2.9 Serial ports

One RJ-45 COM1 port (RS-232 interface) is provided on the front panel. Two COM port is routed to a rear I/O module via the J5 connector.

1.2.10 USB Port

Two USB 2.0 compliant ports with fuse protection are provided. Both ports are routed to front panel connectors on the MIC-3395 and to the rear I/O module via the J5 connector.

1.2.11 LEDs

Four LEDs are provided on the front panel as follows:

One bi-color LED (blue/yellow) indicates hot swap and HDD activity. The blue color indicates that the board may be safely removed from the system, and the yellow color indicates HDD activity.

One LED provides power status. When the LED is green, it means power is provided to the board.

One LED indicates “Master” or “Drone” mode. The green color stands for “Master” mode. When the LED is off, the board is in “Drone” mode.

1.2.12 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control.

The programmable time interval is from 1 to 255 seconds.

1.2.13 Optional Rear I/O Modules

The RIO-3315 is the optional RTM (also known as rear I/O module) for the MIC-3395. It offers a wide variety of I/O features, such as two or four RJ45 LAN ports, two COM ports, two VGA ports, two USB2.0 ports, one P/S2 port, and one Mini-SAS port for the RIO-3315-A1E model. It also comes with on-board features such as two USB2.0, two SATA and four SAS (SATA interfaces) for the RIO-3315-A1E model. RIO-3315-B1E is without on-board SAS controller and with one RJ45 COM port and one DUB 9 pin COM port. In additional, RIO-3315-C1E is with 4 LAN ports, on the front panel. Rear I/O modules are available with two different I/O options:

Table 1.3: RIO-3315 Configuration

RTM Model Number	Rear Panel						On-board Header/Socket/Connector			
	LAN	COM	VGA	PS/2	USB	MiniSAS	USB	SATA	SAS /SATA interface	Conn.
RIO-3315-A1E	2	1	2	1	2	1	2	2	4	J3,J4,J5
RIO-3315-B1E	3	2	2	1	2	-	2	2	-	J3,J4,J5
RIO-3315-C1E	4	1	2	1	2	-	2	2	-	J3,J4,J5

1.2.14 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 60° C (32 ~ 140° F)

Note! *The operating temperature range of the MIC-3395 depends on the installed processor and the airflow through the chassis.*

- **Storage Temperature:** -40 ~ 85° C (-40 ~ 185° F)
- **Humidity:** 95% @ 40° C (non-condensing)
- **Humidity (Non-operating):** 95% @ 60° C (non-condensing)
- **Vibration:** 5 ~ 100Hz, 1.06 Grms with CFast
- **Vibration (Non-operating):** 15 ~ 500Hz, 2 Grms
- **Shock:** 20 G (without on-board 2.5” SATA HDD)
- **Shock (Non-operating):** 50 G
- **Altitude:** 4,000 m above sea level
- **Board size:** 233.35 x 160 mm (6U size), 1-slot (4 TE) wide
- **Weight:** 0.8 kg (1.76 lb)

1.2.15 Compact Mechanical Design

The MIC-3395 has a specially designed CPU heatsink to enable fanless operation. However, forced air cooling in the chassis is needed for operational stability and reliability.

1.2.16 CompactPCI Bridge

The MIC-3395 uses a Pericom PI7C9X130D universal bridge as a gateway to an intelligent subsystem. When configured as a system controller, the bridge acts as a standard transparent PCI Express to PCI/PCI-X Bridge. As a peripheral controller it allows the local MIC-3395 processor to configure and control the onboard local subsystem independently from the CompactPCI bus host processor. The MIC-3395 local PCI subsystem is presented to the CompactPCI bus host as a single CompactPCI device. When the MIC-3395 is in drone mode, the Pericom PI7C9X130D is electri-

cally isolated from the CompactPCI bus. The MIC-3395 receives power from the backplane, supports rear I/O. The Pericom PI7C9X130D PCI bridge offers the following features:

- PCI Interface
  - Full compliance with the PCI Local Bus Specification, Revision 3.0
  - Supports 3.3V PCI signaling with 5V I/O tolerance
- Support transparent mode of operations.
- Support forward bridging
- 64-bit, 66MHz asynchronous operation
- Provides two level arbitration support for 7 PCI Bus masters
- 16-bit address decode for VGA
- Usable in CompactPCI system slot

Please consult the Pericom PI7C9X130D data book for details.

1.2.17 I/O Connectivity

For MIC-3395, the front panel I/O is provided by two RJ-45 Gigabit Ethernet ports, one RJ-45 COM port, two USB 2.0 ports, one VGA connector, and one XMC/PMC knockout.

Its onboard I/O consists of one SATA channel can be connected to a daughter board for 2.5" SATA HDD and a CFast slot. Rear I/O connectivity is available via the following CompactPCI connectors:

- J3: two Gigabit Ethernet links to the backplane for PICMG 2.16 packet switch, two SATA port, one PS/2 port (for keyboard/mouse) and two USB ports on the RTM.
- J4: one Audio output and one DVI.
- J5: Two Gigabit Ethernet LAN ports, two COM ports and one DVI/VGA ports.

1.2.18 XMC / PMC Connectors (Extension Module)

Additional I/O or co-processing functionality is supported by add-on PCI Express Mezzanine Cards (XMC) or PCI Mezzanine Cards (PMC).

MIC-3395 supports one XMC site via PCI Express x8 bus. The XMC slot support one x8 PCI Express gen2 and 10G SFP XMC module of MIC-3666.

MIC-3395supports one PMC connected via 64bit / 66 MHz and 32-bit / 33 MHz PCI bus interface and both 3.3 V and 5 V VIO depend on usage.

1.2.19 Hardware Monitor

One Hardware Monitors (NCT6776F) is available to monitor critical hardware parameters. It is attached to the BMC to monitor CPU temperature and core voltage information.

1.2.20 Super I/O

The MIC-3395 Super I/O device provides the following legacy PC devices:

- Serial port COM1 and COM2 are connected to the rear I/O module or front panel via multiplexer in the FPGA.
- The PS2 (keyboard/mouse) is routed to the rear I/O module.

1.2.21 RTC and Battery

The RTC module keeps the date and time. On the MIC-3395 model the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3 V, 210 mAH).

1.2.22 IPMI

The MIC-3395 uses the Intelligent Platform Management Interface (IPMI) to monitor the health of an entire system. A Renesas H8S/2167 microcontroller provides BMC functionality to interface between system management software and platform hardware. The MIC-3395 implements fully-compliant IPMI 2.0 functionality and conforms to the PICMG 2.9 R1.0 specification. The IPMI firmware is based on proven technology from Avocent. Full IPMI details are covered in Chapter 3.

1.3 Functional Block Diagram

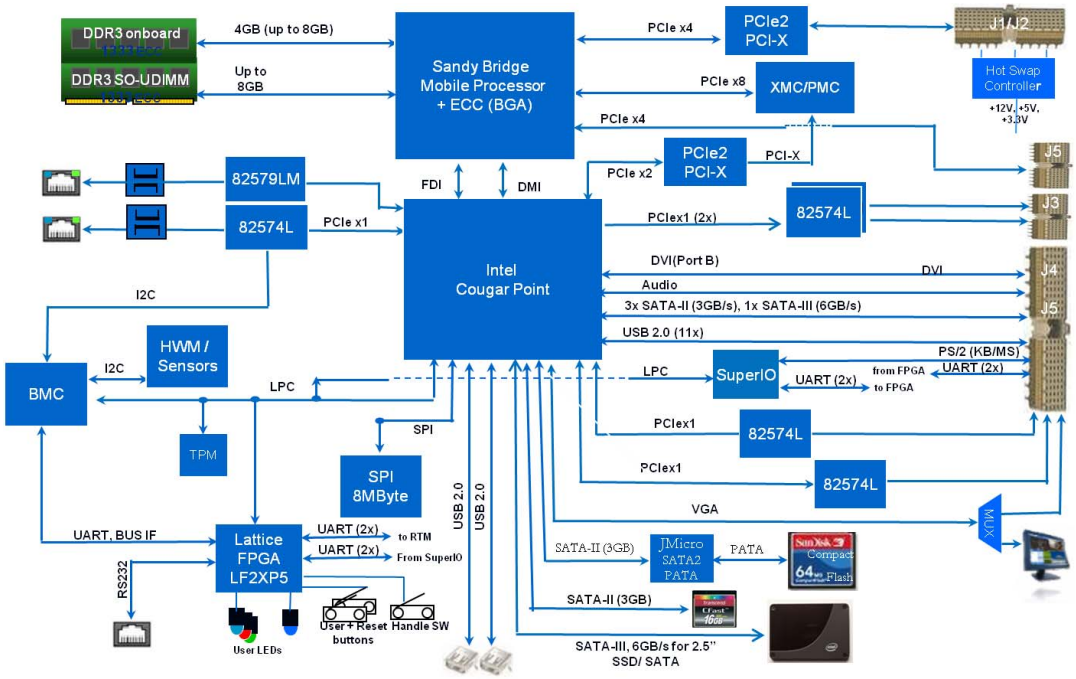


Figure 1.1 MIC-3395 Functional Block Diagram

1.4 Jumpers and Switches

Table 1.4 and table 1.5 list the jumper and switch functions. Read this section carefully before changing the jumper and switch settings on your MIC-3395 board.

Table 1.4: MIC-3395 Jumper Descriptions

Number	Function
CN12	Clear CMOS
JP11	PMC VIO
JP3	LCD Power for reserved TBD

Table 1.5: MIC-3395 Switch Descriptions

Number	Function
SW5	BMC Reset/Platform Reset
SW1-2	BMC Firmware Programmable/Console Setting (with SW2 together)
SW1-1	PCI Bridge Master/Drone Mode
SW2	Front COM & RTM COM1/COM2 ports selection for BMC/SIO UART, or BMC Firmware Programmable/Console Setting

1.4.1 Clear CMOS (CN12)

This jumper is used to erase CMOS data. Follow the procedures below to clear the CMOS.

1. Turn off the system.
2. Close jumper CN12 for about 3 seconds.
3. Set jumper CN12 as Normal.
4. Turn on the system. The BIOS is reset to its default setting.

Table 1.6: CN12 Clear RTC

	Closed	Clear RTC
Default	Open	Normal

1.4.2 PMC VIO Setting (JP11)

This jumper is used for setting the PMC IO voltage.

1. JP11 (1-2) for +3.3 V
2. JP11 (2-3) for +5 V

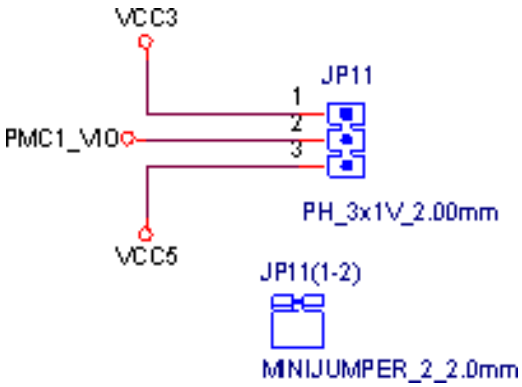
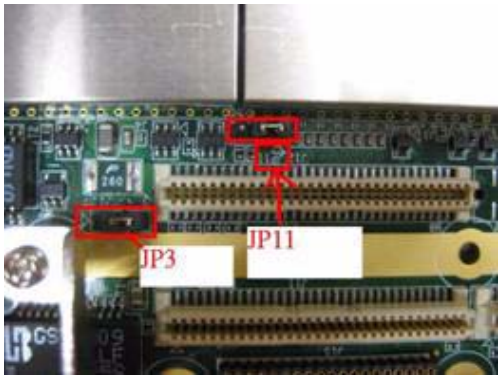


Figure 1.2 JP11 for PMC VIO (+3.3 V or +5 V)

1.4.3 LCD Power Setting (JP3)

Table 1.7: JP3 LCD Power

	Voltage	Setting
Default	3.3 V	JP3 (2-3)
	5 V	JP3 (1-2)



1.4.4 Switch Settings

Table 1.8: SW5 BMC Reset Button & Platform Reset Button	
SW5-2 (top)	BMC Reset
SW5-1 (bottom)	Platform Reset

Table 1.9: SW1-2 & SW2-1 BMC Program or Console		
Default	BMC Console	SW1-2 SW2-1 ON 1 2 ON 1 2 3 4
	MC Program	SW1-2 SW2-1 ON 1 2 ON 1 2 3 4

When either front panel COM, RTM COM1 or RTM COM2 is connected to the BMC, the BMC firmware can be re-programmed by setting switch 1 and switch 2 to “BMC Program” mode.

Table 1.10: SW1-1 PCI Bridge Master/Drone Mode		
Default	Master Mode	SW1-1 ON 1 2
	Drone Mode	SW1-1 ON 1 2

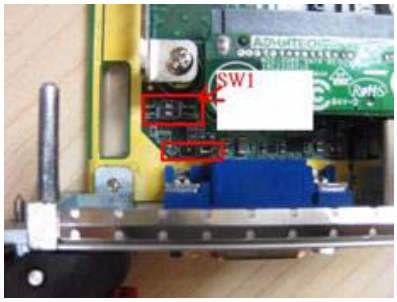
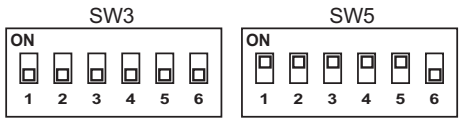


Table 1.11: SW2 Front COM & RTM COM1/COM2 Ports Selection for BMC/SIO UART		
Default	Front COM for BMC RTM COM1 for SIO COM1 RTM COM2 for SIO COM2	SW2 ON 1 2 3 4
	Front COM for SIO COM1 RTM COM1 for BMC RTM COM2 for SIO COM2	SW2 ON 1 2 3 4
	Front COM for SIO COM2 RTM COM1 for SIO COM1 RTM COM2 for BMC	SW2 ON 1 2 3 4

1.4.5 RIO-3315-A1E Switch Setting

Table 1.12: SW4 External Mini-SAS Port/Internal SAS Interface		
Default	External Mini-SAS 4x Port	1 2 3 4 ON
	Internal SATA ports 1 (SAS Port0) 2 (SAS Port1) 3 (SAS Port2) 4 (SAS Port3)	1 2 3 4 ON

Table 1.13: SW3 & SW5 COM2		
Default	RS232	SW3 ON 1 2 3 4 5 6 SW5 ON 1 2 3 4 5 6
	RS422	SW3 ON 1 2 3 4 5 6 SW5 ON 1 2 3 4 5 6

Table 1.13: SW3 & SW5 COM2	
RS485	

This switch is only available for the RIO-3315-A1E (supports SAS function) model.

1.5 Connector Definitions

Table 1.14 lists the function of each connector and Figure 1.3 and 1.4 illustrate each connector location.

Table 1.14: MIC-3395 Connector Descriptions

Number	Function
CNSATA1	SATA HDD daughter board
J15	XMC
CNDIMM	SODIMM socket
J1/J2	Primary CompactPCI bus
J3/J4/J5	Rear I/O transition

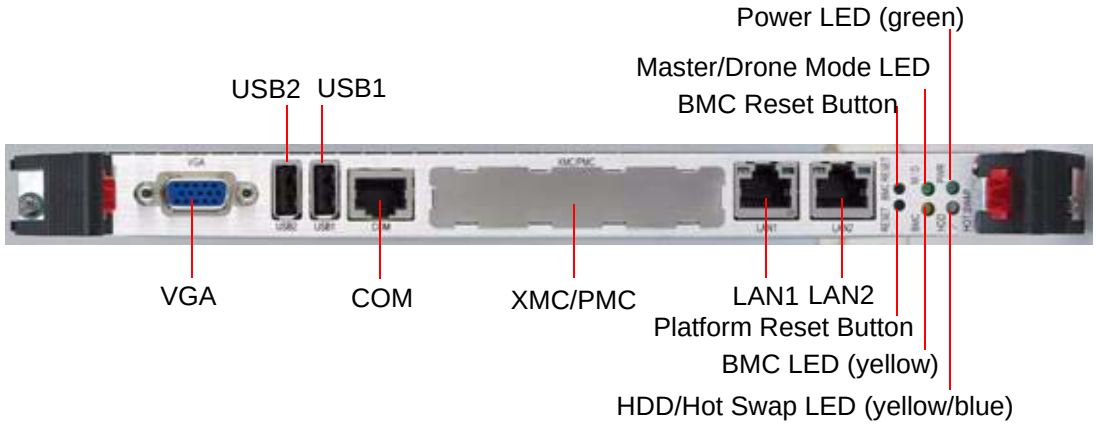


Figure 1.3 MIC-3395 Front Panel Ports, Indicators and Buttons

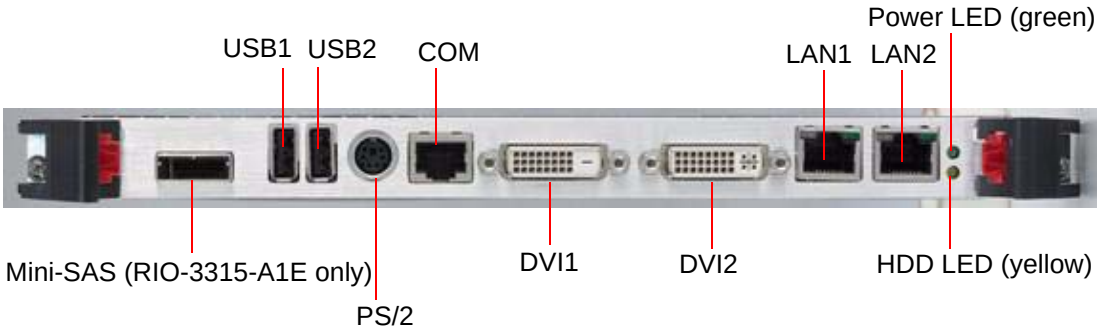


Figure 1.4 RIO-3315 Front Panel Ports and Indicators

1.5.1 USB Connectors

The MIC-3395 provides up to fourteen Universal Serial Bus (USB) 2.0 channels. Two USB ports, CNUSB1 and CNUSB2, are on the front panel. One is routed to an on-board USB flash disk. Eleven other USB channels are routed to rear I/O via the J3/J5 connector. Two on the panels, the other two are on-board connectors. However, RIO-3315-A1E supports two on-board USB ports. The USB interface provides complete plug and play, hot attach/detach for up to 127 external devices. The MIC-3395 USB interface complies with USB specification R2.0 and is fuse protected (5 V @ 1.1 A). The USB interface can be disabled in the system BIOS setup. The USB controller default is set to “Enabled”.

1.5.2 Serial Ports

The MIC-3395 provides one serial port and the RIO-3315 provides two serial ports. They are available as RS-232 interfaces via RJ-45 connectors on the front panel. An RJ-45 to DB-9 adaptor cable is provided in the MIC-3395 accessories to facilitate connectivity to external console or modem devices. The BIOS Advanced Setup program covered in Chapter 2 provides a user interface for features such as enabling or disabling the ports and setting the port address. Many serial devices implement the RS-232 standard in different ways. If you have problems with a serial device, be sure to check pin assignments on Table 1.11 for the connectors. The IRQ and address range for these ports are fixed. However, if you wish to disable the port or change these parameters later, you can do this in the system BIOS setup.

1.5.3 Ethernet Configuration

The MIC-3395 is equipped with two high performance, PCI-Express based, network interface controllers which provide fully compliant IEEE802.3 10/100/1000 Base-TX Ethernet interfaces; QM67 built-in PHY chip which also provides 10/100/1000Base-TX Ethernet interface. Users can choose the LAN1 and LAN2 either via the front panel RJ-45 connectors or the LAN1 and LAN2 on the rear I/O module. Furthermore, the MIC-3395 supports the PICMG 2.16 Packet Switching Backplane Specification via the J3 connector.

1.5.4 SATA Daughter Board Connector (CN7 and Extension Module)

The MIC-3395 provides one SATA interface; a daughter board with SATA HDD socket is attached to connector CN7 for optional HDD. If required, and by request, an additional SATA interface may be connected to XTM.

1.5.5 System Rest and BMC Reset Button

The MIC-3395 provides a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry. It does not reset the system management (IPMI) related circuitry. A separate BMC reset button on the front panel is provided for the BMC and related hardware.

1.5.6 Mini-SAS Connector (Rear I/O)

The RIO-3315-A1E provides one SAS interface integrates with a 3.0 Gbit/s SAS/SATA controller that is compliant with the Fusion-MPT (Message Passing Technology) architecture, provides an eight-lane PCI Express interface, and supports integrated RAID technology. The controller is routed to a x4 mini-SAS connector on the front panel for a mini-SAS (SFF8088) cable when connecting externally; or to four on-board SATA Gen. 2 ports by adjusting SW1 switch setting. Figure 1.5, 1.6 and 1.7 describe SAS configurations.

- Blades, RTMs and drives must be installed in the same chassis

- Two drives are shared by two blades when executing RAID 1
- Use 2 pcs 1:2 cable for internal connectors (1x SFF8482, 2x SATA, 1x Power)

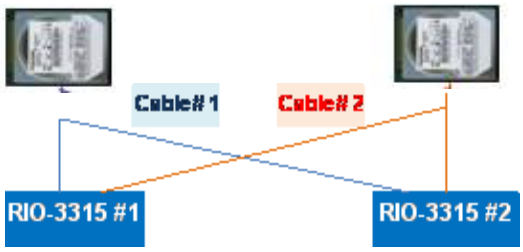


Figure 1.5 SAS Configuration Scenario 1 - Shared Drives

- Connect to external RAID array
- 1pc mini-SAS cable for external connector (2x SFF8088)

Figure 1.6 SAS Configuration Scenario 2 - External Drive Array

- RIO-3315 connects to one drive per port
- 1pc 1:1 cable for internal connector per drive (1x SFF8482, 1x SATA, 1x Power)

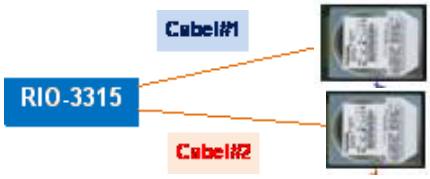


Figure 1.7 SAS Configuration Scenario 3 - Individual Drives

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your CompactPCI chassis before you work on it. Don't touch any components on the CPU board or other boards while the CompactPCI chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installation Steps

The MIC-3395 contains electrostatically sensitive devices. Please discharge your body and clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an anti-static workbench.

1.7.1 HDD Installation Steps

The MIC-3395 supports 2.5” SATA hard disk drive. The SATA HDD daughter board is not assembled on the MIC-3395. The following steps illustrate the installation of the SATA HDD.

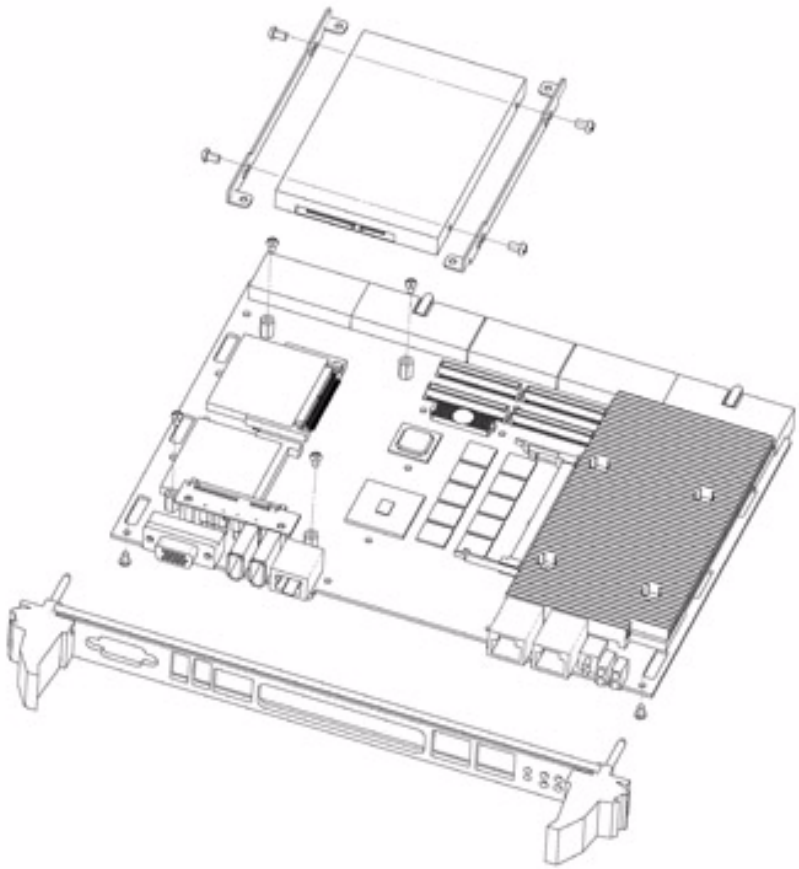


Figure 1.8 Complete Assembly of MIC-3395 with SATA HDD

1. Align the HDD bracket on the side of HDD and fasten 4pcs M2.5 screw on the bracket.

Figure 1.9 Fasten Screws on the SATA HDD Bracket

2. Put the SATA HDD with bracket on the post and insert SATA HDD into SATA connector.

Figure 1.10 Insert SATA HDD into SATA Connector

1.8 Battery Replacement

The Battery model number is CR2032M1S8-LF, a 3 V, 210 mAh battery. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact with your local salesperson to check availability.

1750129010 - BATTERY 3V/210 mAh with WIRE ASS'Y CR2032M1S8-LF.

1.9 Software Support

Windows 7, Windows XP, Windows 2000, Windows 2003 and Red Hat Enterprise Linux have been fully tested on the MIC-3395. Please contact your local sales representative for details on support for other operating systems.

Chapter 2

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS has been customized and integrated into zillions of industrial and embedded motherboards for over a decade. This section describes the BIOS which has been specifically adapted to the MIC-3395. With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of the MIC-3395. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-3395 setup screens.

Figure 2.1 Setup Program Initial Screen

2.2 BIOS Setup

The MIC-3395 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features.

The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

When the power is turned on, press the <Del> button during the BIOS POST (Power - On Self Test) to access the CMOS SETUP screen.

Control Keys	
< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select Item
<Esc>	Main Menu - Quit and not save changes into CMOS Sub Menu - Exit current page and return to Main Menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for Setup Sub Menu
<F2>	Item Help
<F5>	Load Previous Values

<F7>	Load Setup Defaults
<F10>	Save all CMOS changes

2.3 Entering Setup

Turn on the computer, and there should be a POST (Power-On Self Test) screen that shows the BIOS supporting the CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that the CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

2.3.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

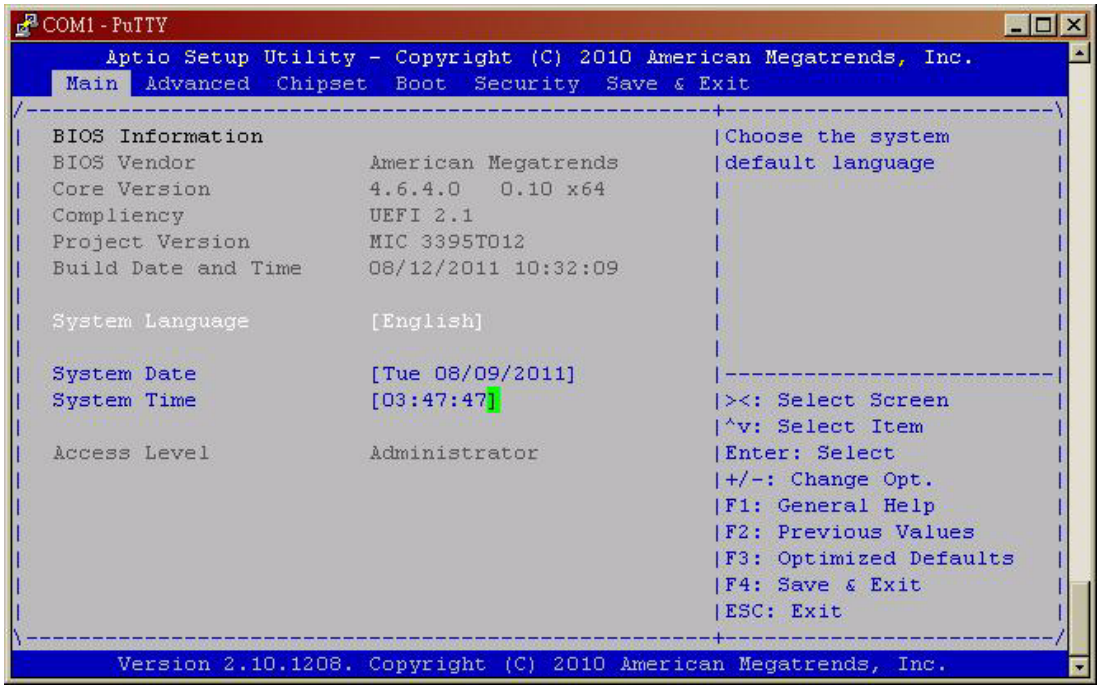


Figure 2.2 Main Setup Screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured whilst options in blue can. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

2.3.1.1 System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.3.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIC-3395 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

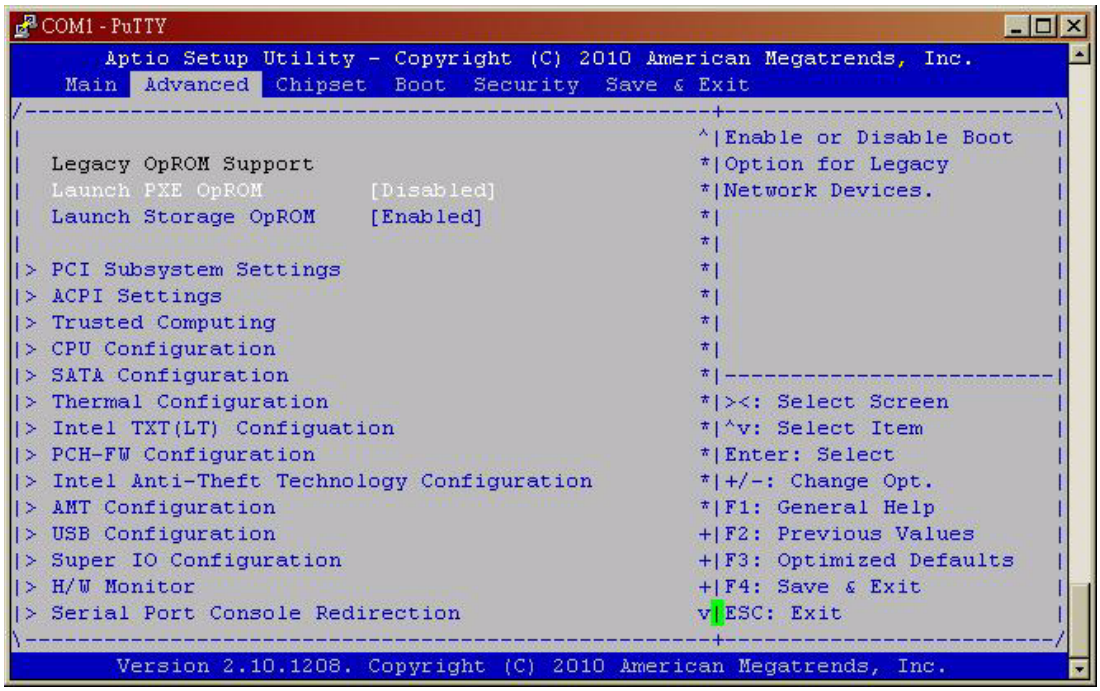
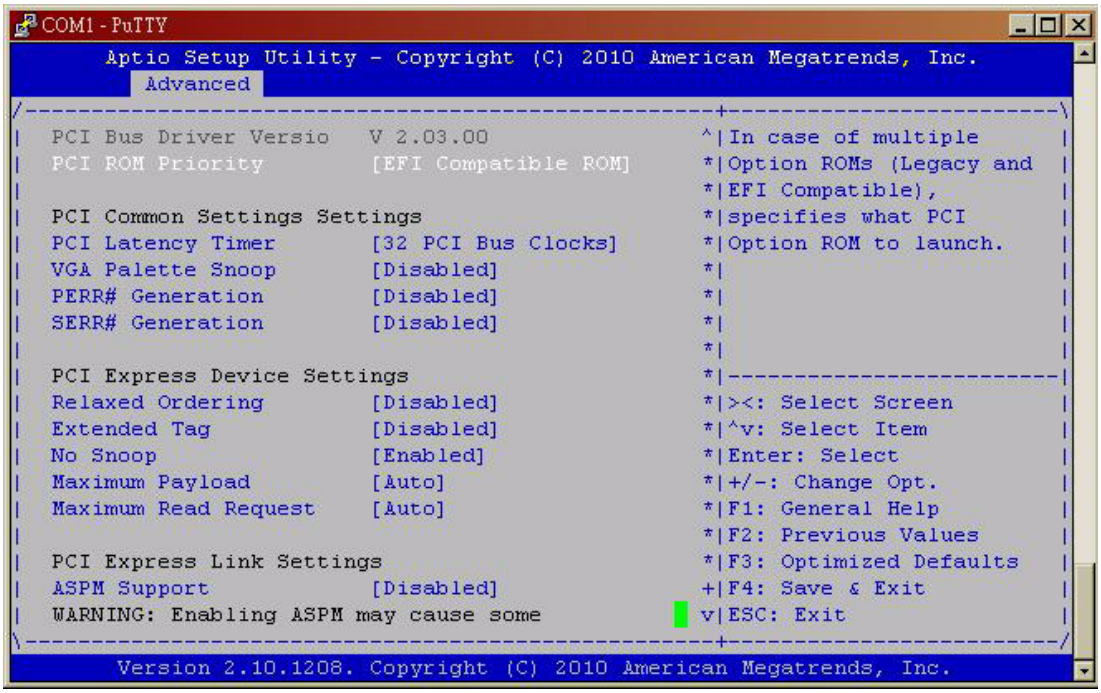


Figure 2.3 Advanced BIOS Features Setup Screen

2.3.2.1 PCI Subsystem Setting



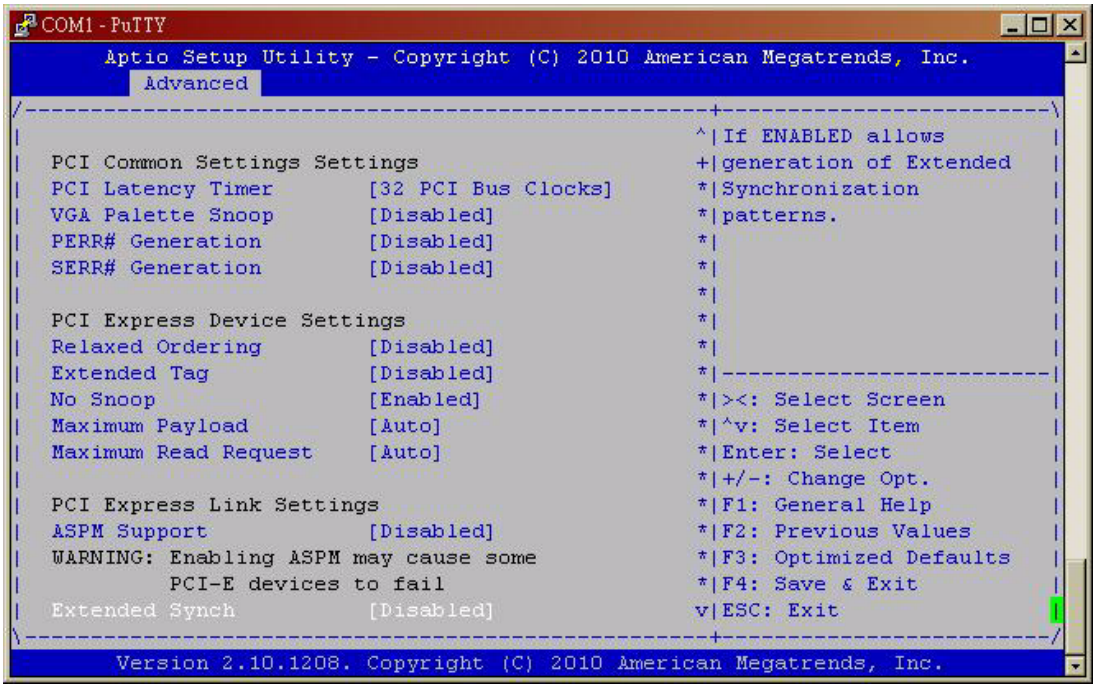


Figure 2.4 PCI Setting

- **PCI ROM Priority**
  In case of multiple option ROMs (Legacy and EFI Compatible), specifies what PCI option ROM to launch.
- **Extended Synch**
  "Enabled" allows generation of extended synchronization patterns.

2.3.2.2 ACPI Setting

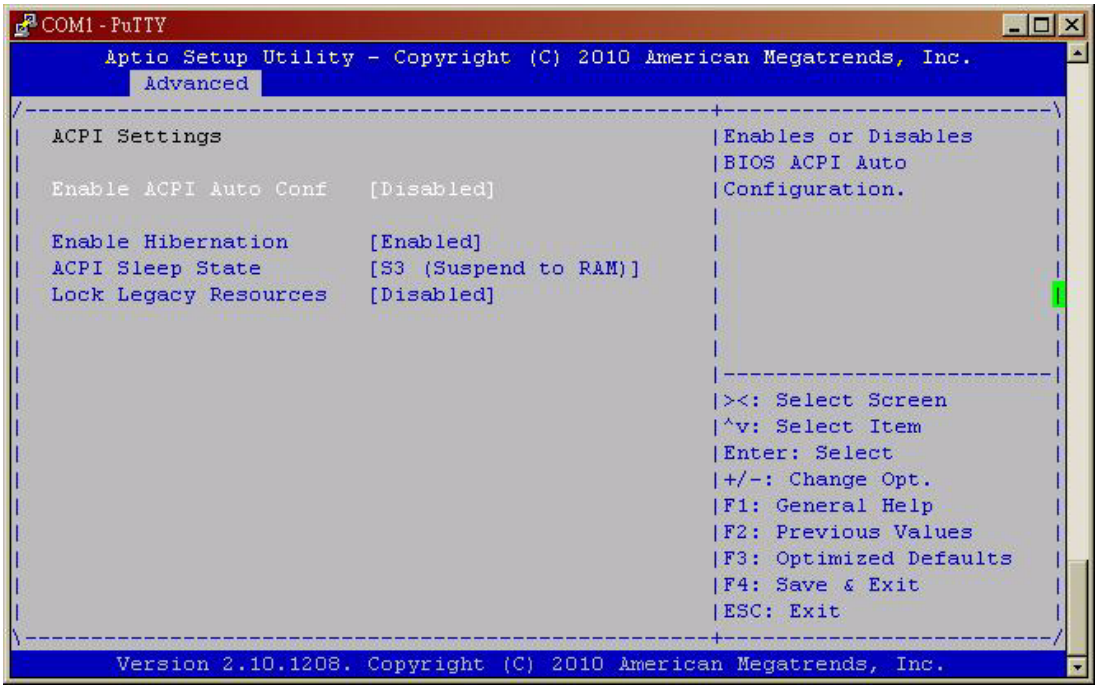


Figure 2.5 ACPI Settings

- **Enable ACPI Auto Configuration**
  Enable or disable BIOS ACPI auto configuration.

- **Make System with Fixed Time**
- **Power On by Modem**

  This allows the system to be awakened from an ACPI sleep state by a wake-up signal from a modem, which supports wake-up function.

2.3.2.3 CPU Configuration

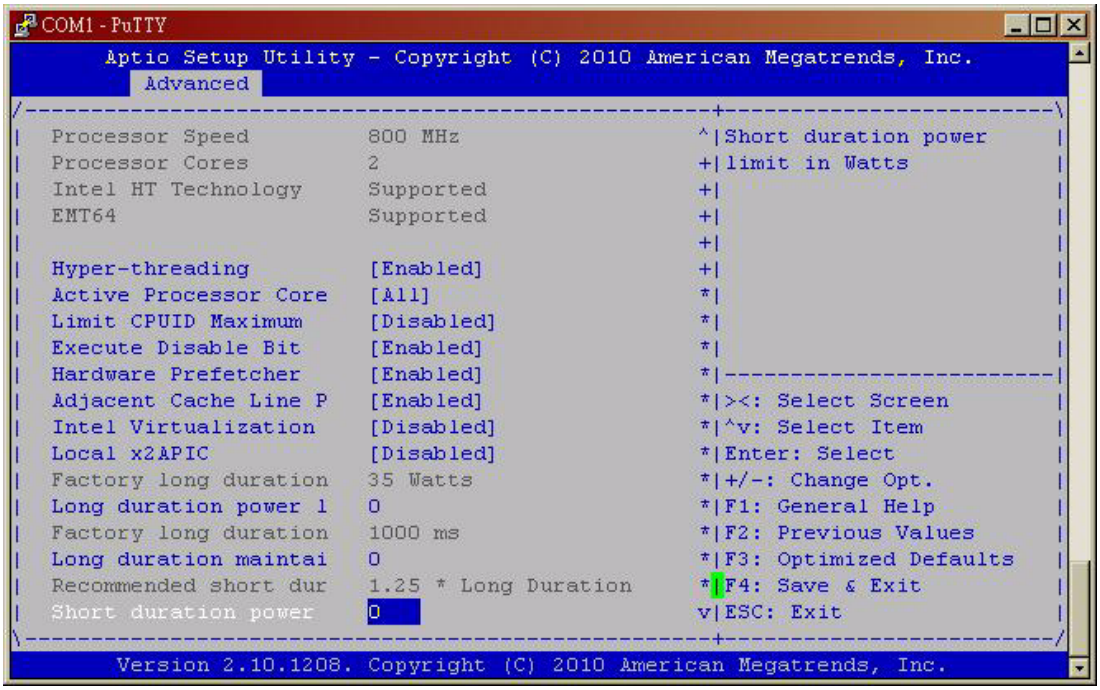


Figure 2.6 CPU Configuration

- **Hyper-Treading**

  This item allows you to enable or disable Intel Hyper Threading technology.

- **Active Processor Core**
  It allows you to choose the number of CPU cores to activate in each processor package.
- **Limit CPUID Maximum**
  This item allows you to limit CPUID maximum value.
- **Execute Disable Bit**
  This item allows you to enable or disable the No-Execution page protection technology.
- **Hardware Prefetcher**
  The processor fetches data and instructions from the memory into the cache are likely to be required in the near future. This reduces the latency associated with memory reads.
- **Adjacent Cache Line Prefetcher**
  This item allows users to enable or disable the adjacent cache line prefetcher feature.
- **Intel Virtualization Tech**
  Intel Virtualization Technology (Intel VT) is a set of hardware enhancements to Intel server and client platforms that provide software-based virtualization solutions.
  Intel VT allows a platform to run multiple operating systems and applications in independent partitions, allowing one computer system can function as multiple virtual systems.

2.3.2.4 SATA Configuration

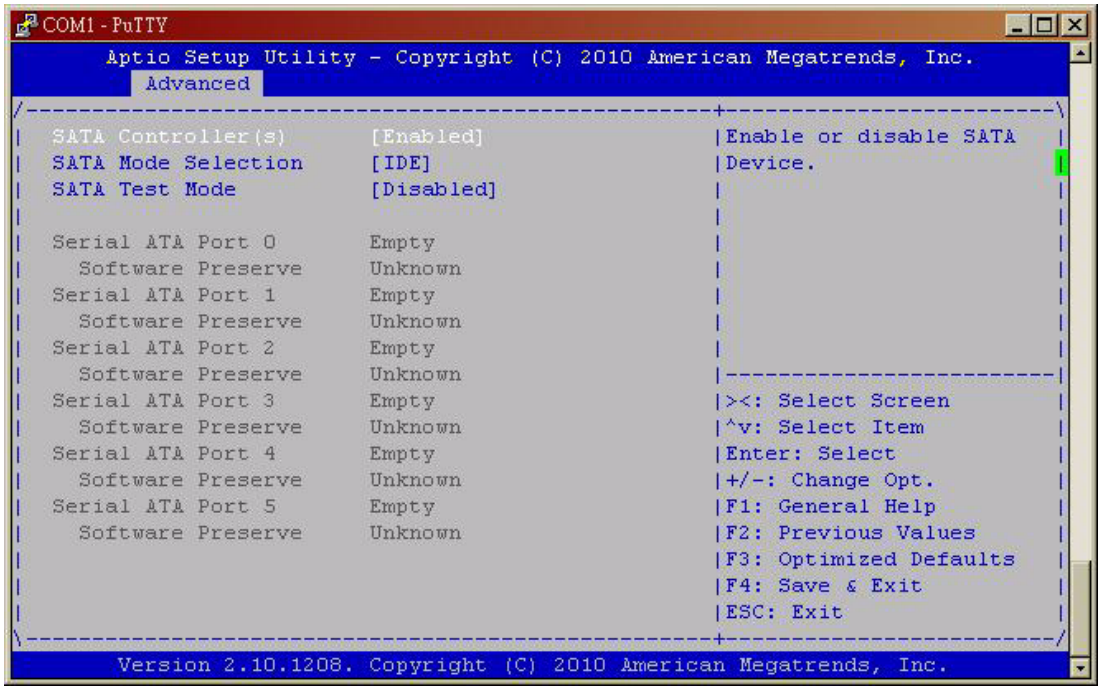


Figure 2.7 SATA Configuration

- **SATA Controller**
  This item appears only by setting SATA mode to "IDE Mode".
- **[Disabled]**
  Disable SATA function.

- **SATA mode**
  This can be configured as IDE or AHCI mode.
- **Disable**
  Disable the SATA function.
- **IDE mode**
  Set to [IDE mode] when you want to use the serial ATA hard disk drives as Parallel ATA physical storage devices.
- **ACHI mode**
  Set to [AHCI mode] when you want the SATA hard disk drives to use the AHCI (Advanced Host Controller Interface). The AHCI allows the onboard storage driver to enable advanced serial ATA features that increase storage performance on random workloads by allowing the drive to internally optimize the order of commands.

2.3.2.5 Intel TXT Configuration

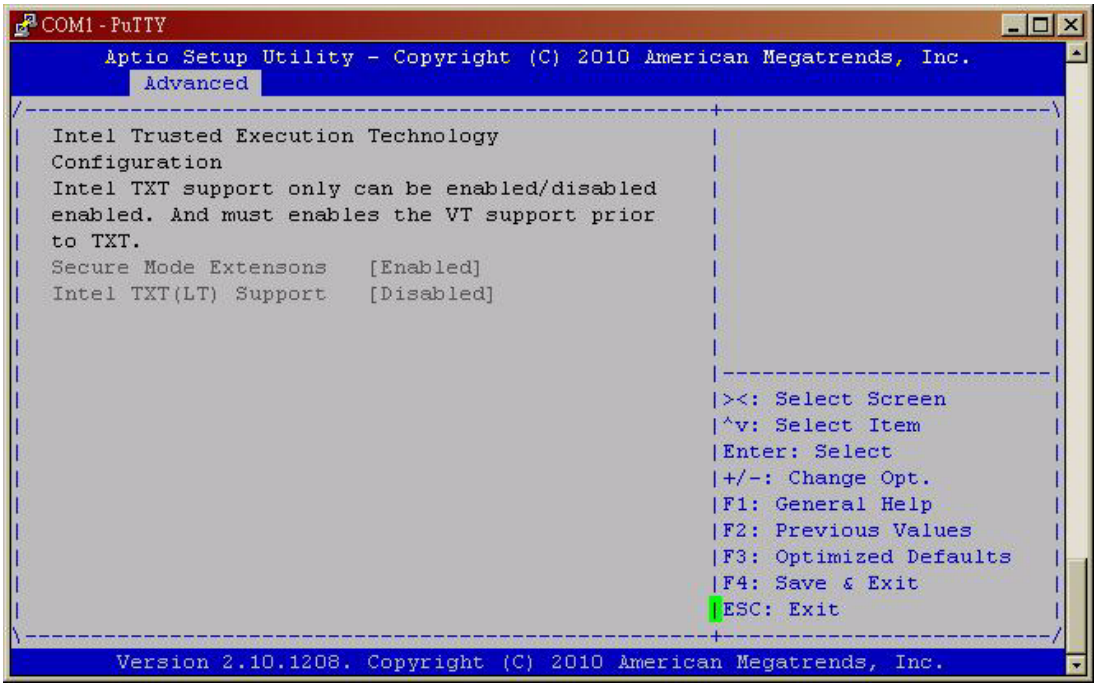


Figure 2.8 Intel TXT Configuration

- **Secure Mode Extension (SMX)**
- **Intel TXT Configuration**
  This item allows to enabling or disabling Intel Trusted Execution Technology.

2.3.2.6 USB Configuration

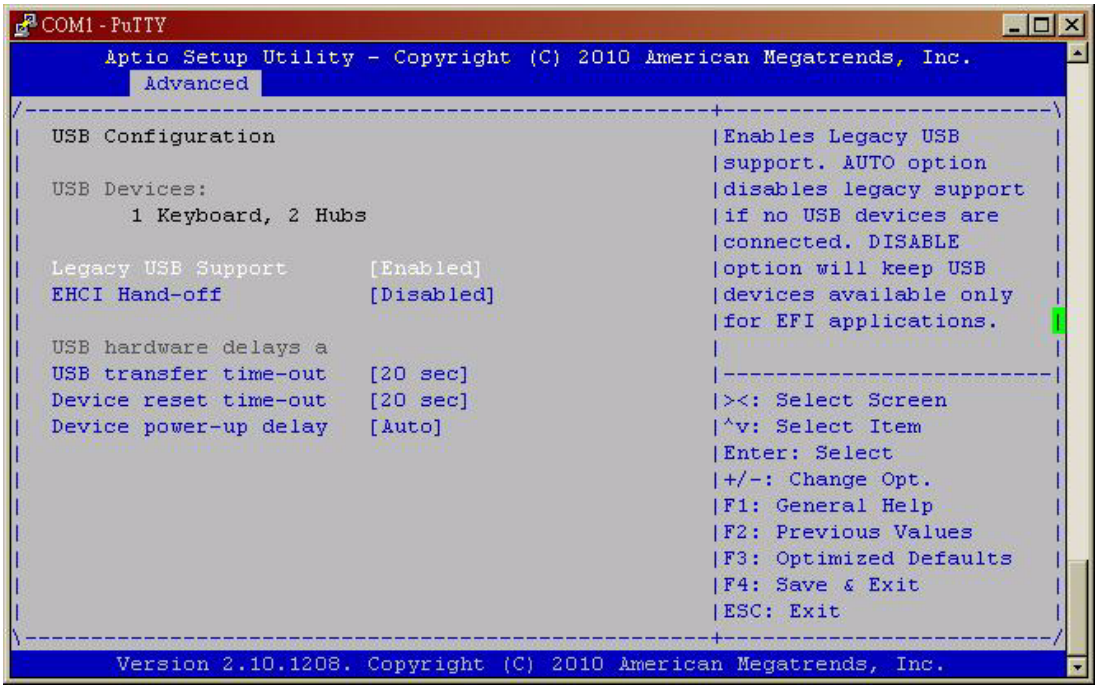


Figure 2.9 USB Configuration

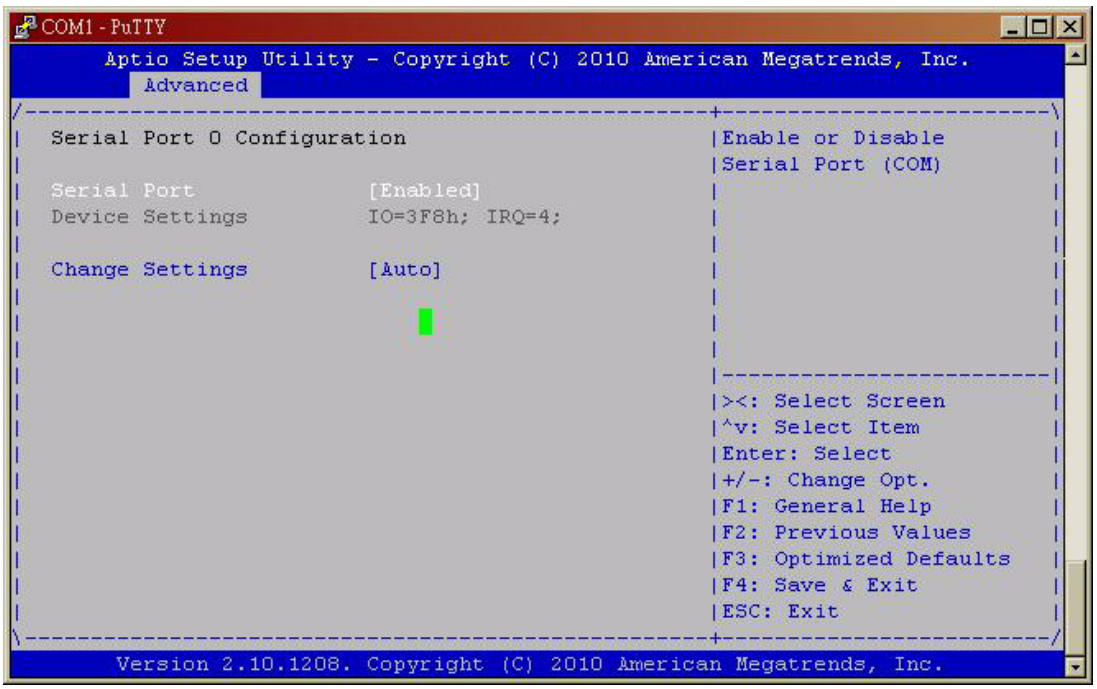
- **Legacy USB Support**
  Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.
- **EHCI Hand-off**
  This is a workaround item for any OS without EHCI hand-off support.
- **Device Reset time-out**
  USB mass storage device start unit command time out.
- **Mass Storage Devices**
  Shows the USB mass storage devices' detailed information.

2.3.2.7 Super IO Configuration

Figure 2.10 Super IO Configuration

- **Serial Port 1/2 Configuration**

  For serial port 1/2, IRQ/IO mode resource configuration, users can choose IRQ, IO and MODE.



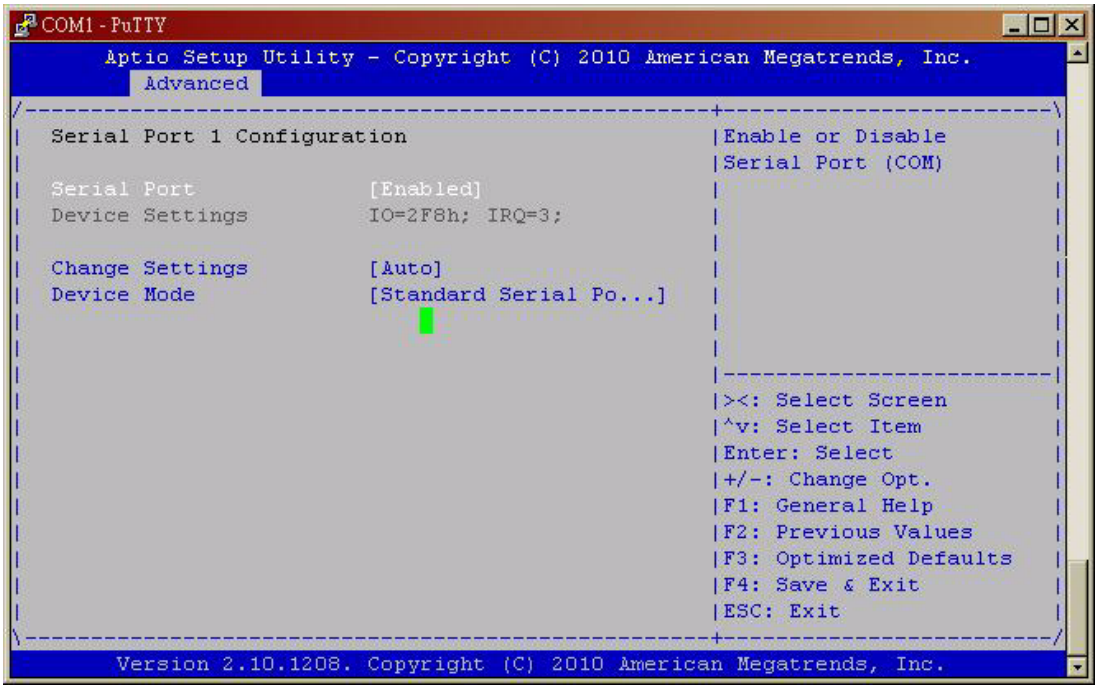


Figure 2.11 Serial Port 1/2 Configuration

CIR Controller Configuration

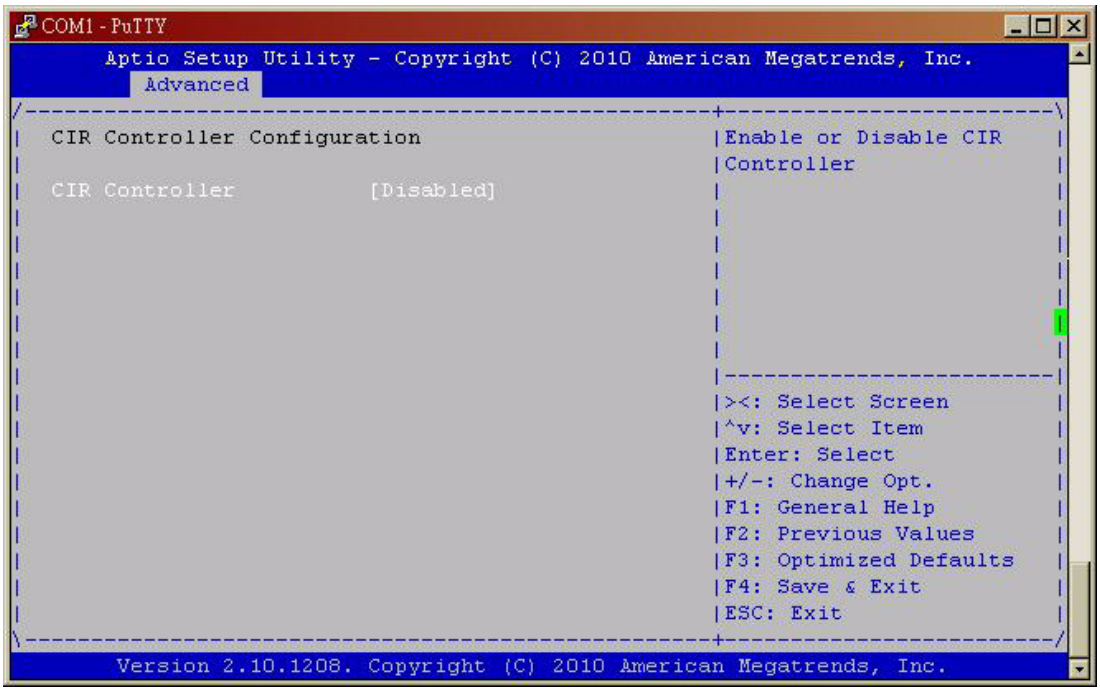


Figure 2.12 CIR Controller Configuration

2.3.2.8 H/W Monitor

System temperature, CPU temperature and voltage status can be checked up on hardware health.

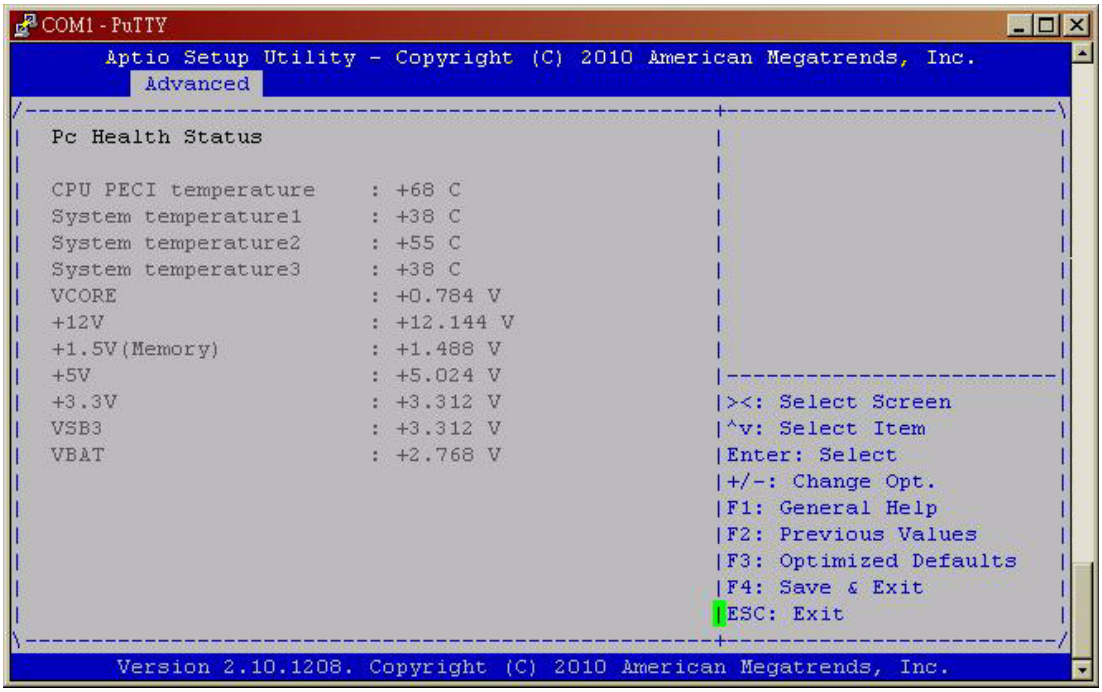


Figure 2.13 PC Health Status

2.3.2.9 Console Redirection Setting

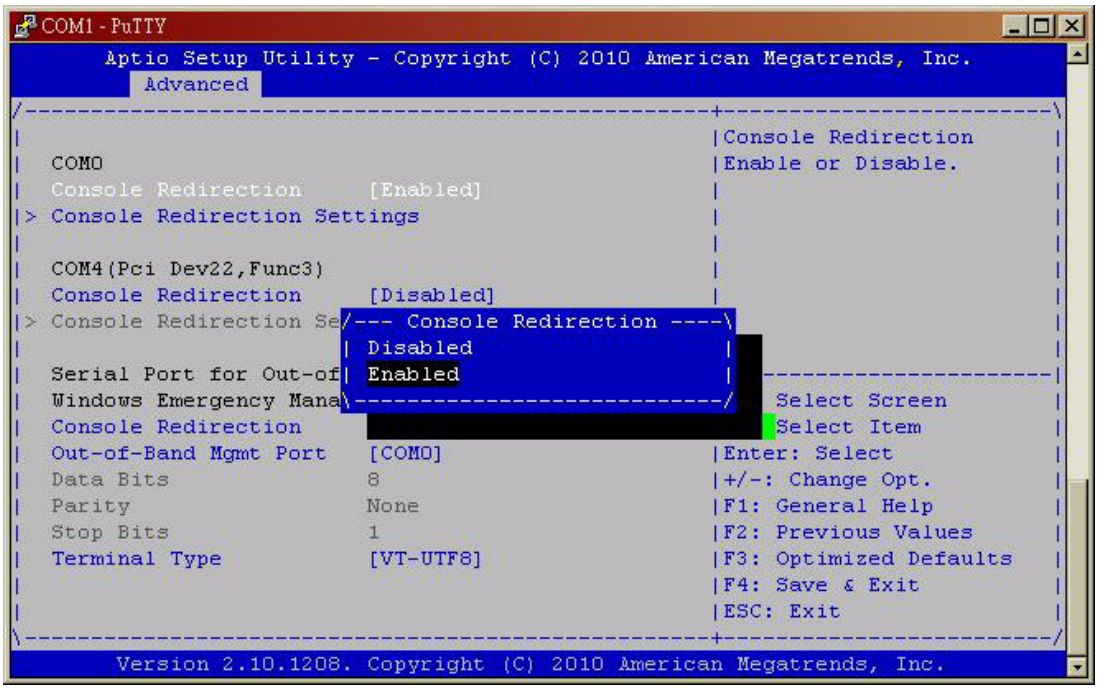


Figure 2.14 Console Redirection Setting

- **Console Redirection**

  This item allows users to enable or disable console redirection or Microsoft Windows Emergency Management Services (EMS).

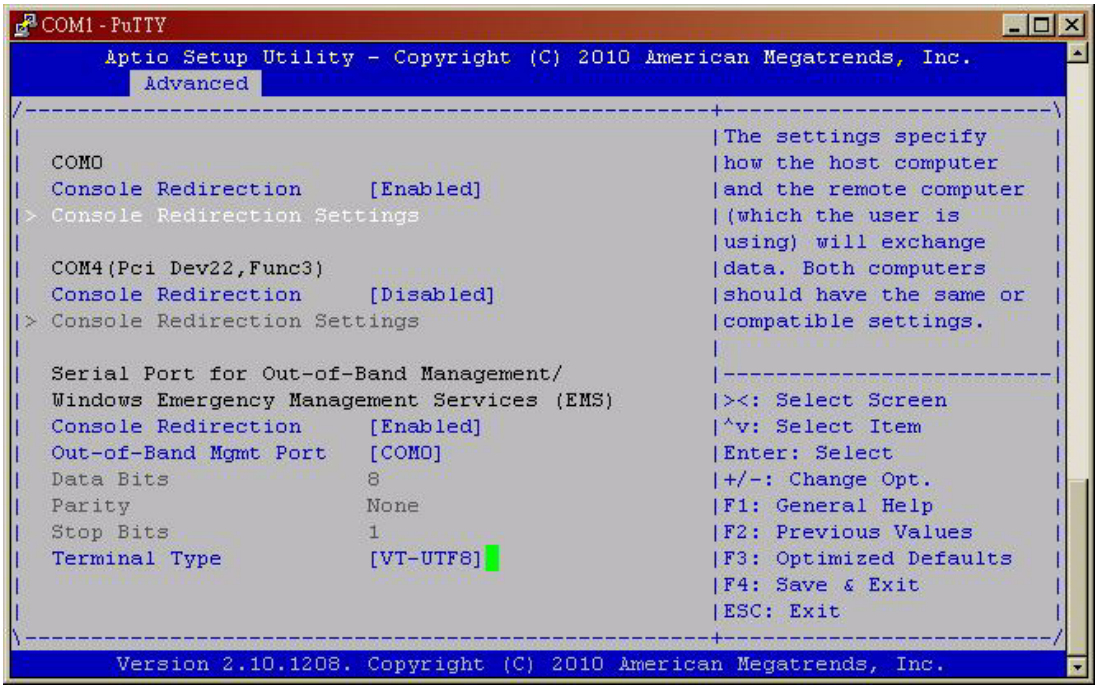


Figure 2.15 Out-of-Band Mgmt Port

- **Out-of-Band Mgmt Port**

  Select the port for Microsoft Windows Emergency Management Services (EMS) to allow for remote management of a Windows Server OS.

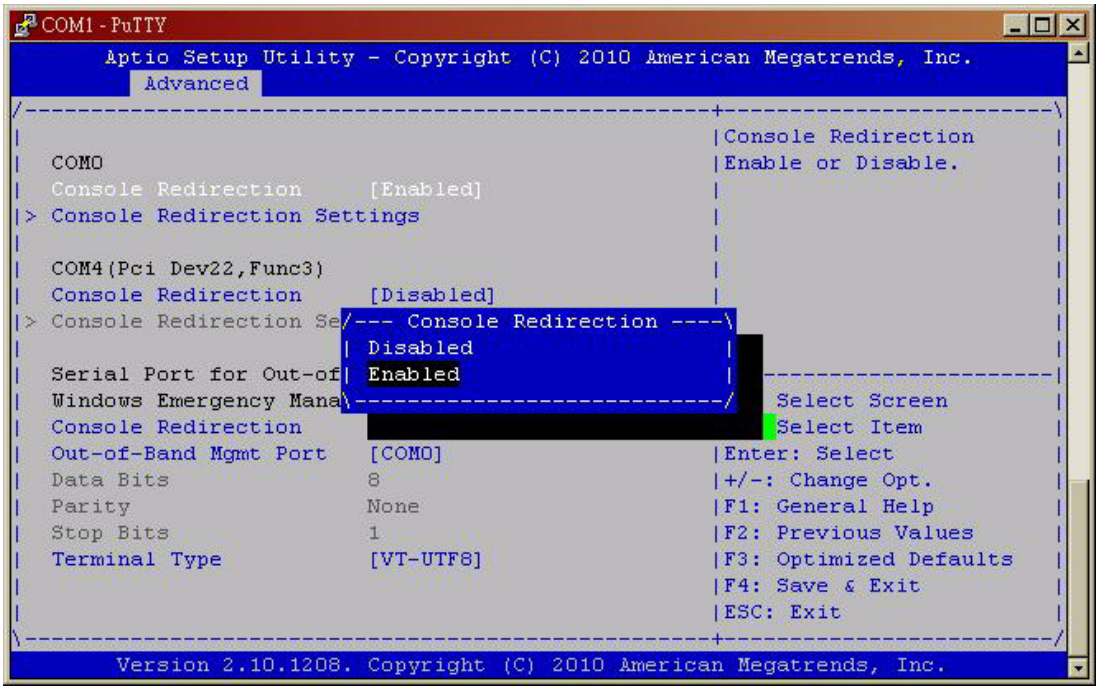


Figure 2.16 Terminal Type

- **Terminal Type**

  VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

2.3.2.10 AMT Configuration

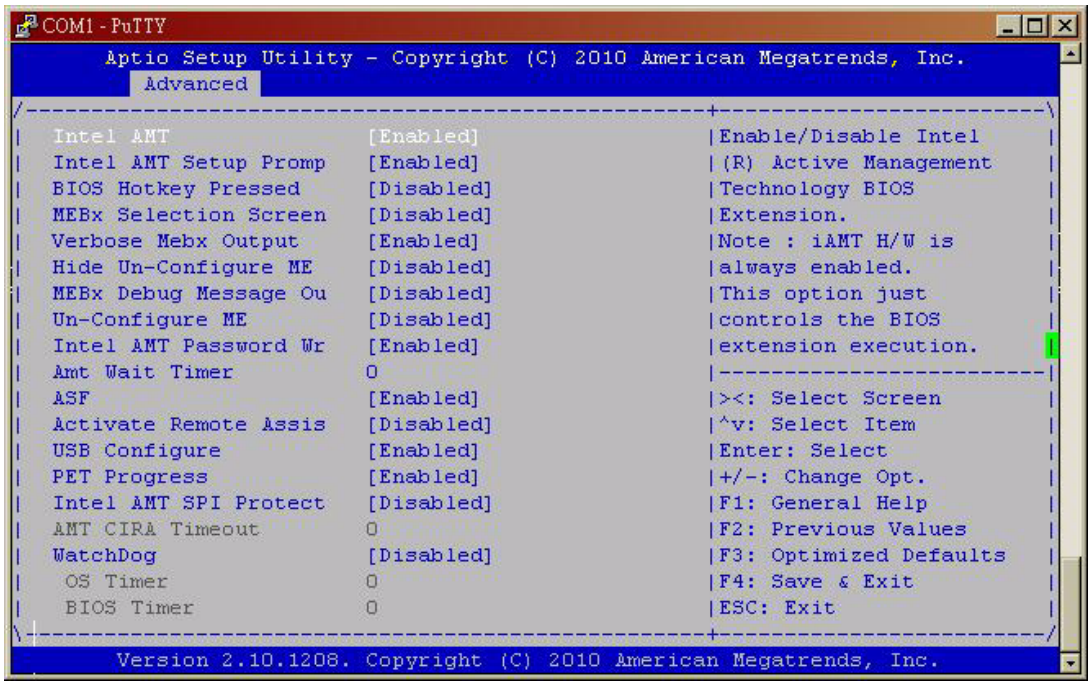


Figure 2.17 AMT Configuration

- **Intel AMT**
  This item allows users to enable or disable Intel AMT BIOS extension.
- **Intel AMT Setup Prompt**
  This item allows users to enable or disable Intel AMT Setup prompt.
- **BIOS Hotkey Pressed**
  This item allows users to enable or disable BIOS hotkey pressed.
- **MEBx Selection Screen**
  This item allows users to enable or disable MEBx selection screen.
- **Verbose MEBx Output**
  This item allows users to enable or disable MEBx Output.
- **Hide un-configuration ME confirmation**
  This item allows users to hide un-configured ME without password confirmation prompt.
- **MEBx Debug Message Output**
  This item allows users to enable or disable MEBx debug message.
- **Un-Configured ME**
  This item allows users to Un-configured ME without password.
- **Intel AMT Password Write Enabled**
  This item allows users to enable or disable Intel AMT password write.
- **Amt Wait Timer**
  Set timer to wait before sending ASF_GET_BOOT_OPTIONS.
- **Activated Remote Assistance Process**
  This item allows users to enable or disable Alert Specification Format.
- **USB Configure**
  This item allows users to enable or disable USB Configure Function.

- **PET Progress**
  This item allows users to enable or disable PET event progress to receive PET events or not.
- **Intel AMT SPI Protected**
  This item allows users to enable or disable Intel AMT SPI write protect.
- **AMT CIRA Timeout**
  OEM defined time out for MPS connection to be established.
- **Watchdog**
  This item allows users to enable or disable WatchDog Timer.
- **OS Timer**
  Sets OS Watchdog Timer.
- **BIOS Timer**
  Set BIOS Watchdog timer.
- **Intel Anti-Theft Technology**
  This item allows users to enable or disable Intel® Anti-Theft Technology, which helps stop laptop theft by making computers useless to thieves via immediate laptop shut down.

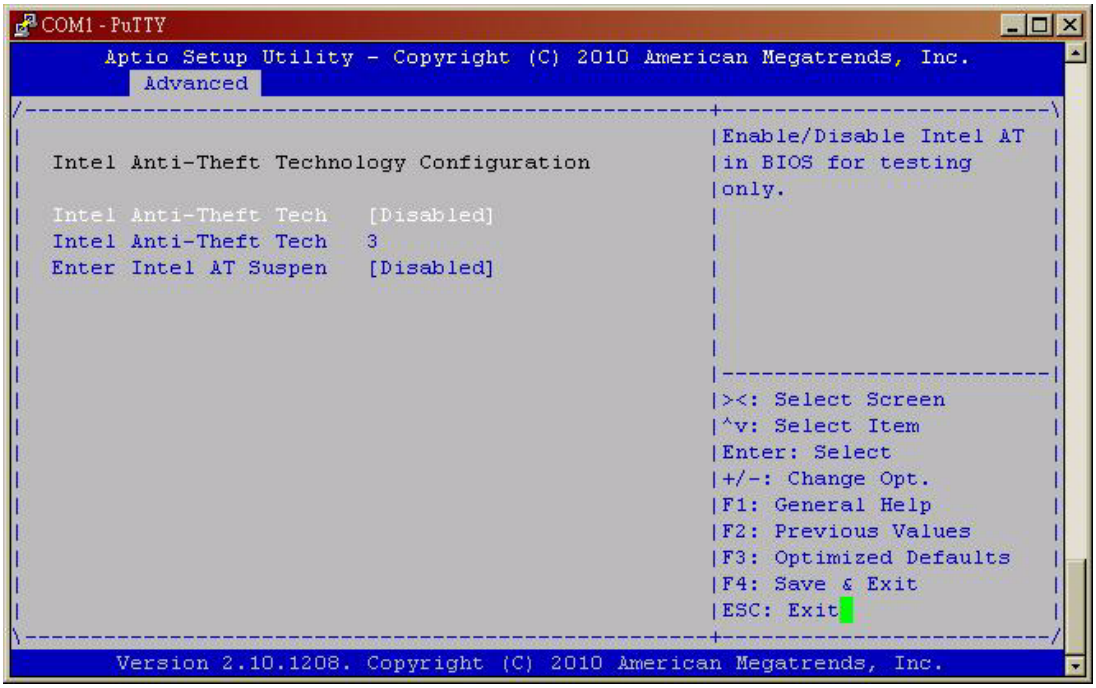


Figure 2.18 Intel Anti-Theft Technology

- **ME FW Image Re-Flash**
  This item allows users to enable or disable ME FW image re-flash function.

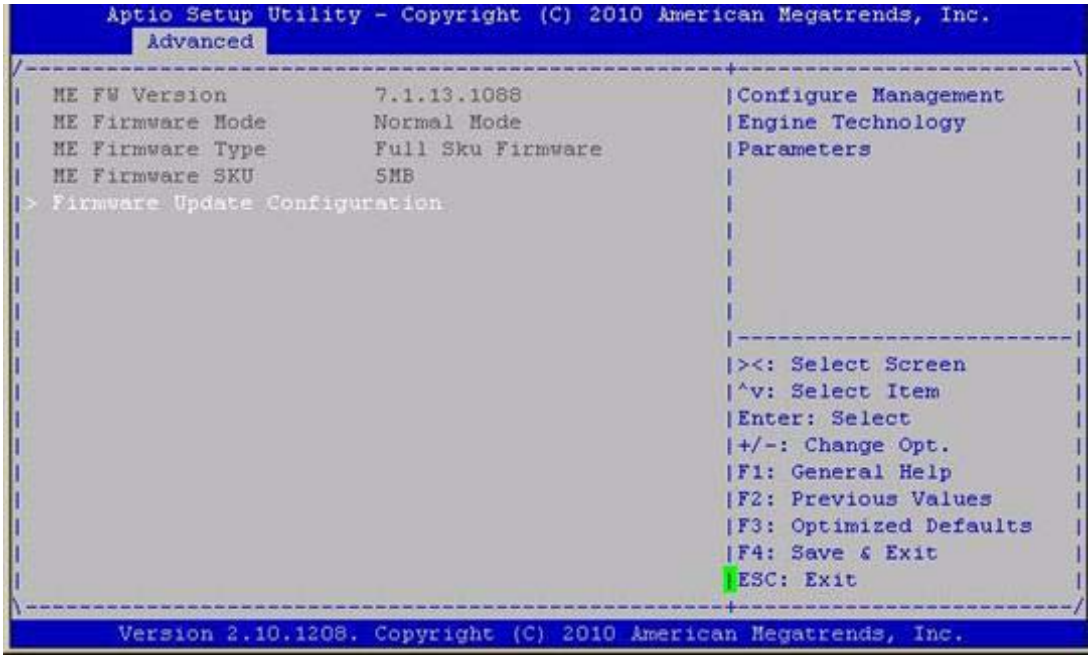


Figure 2.19 ME FW Image Re-Flash

2.3.2.11 Switchable Graphics

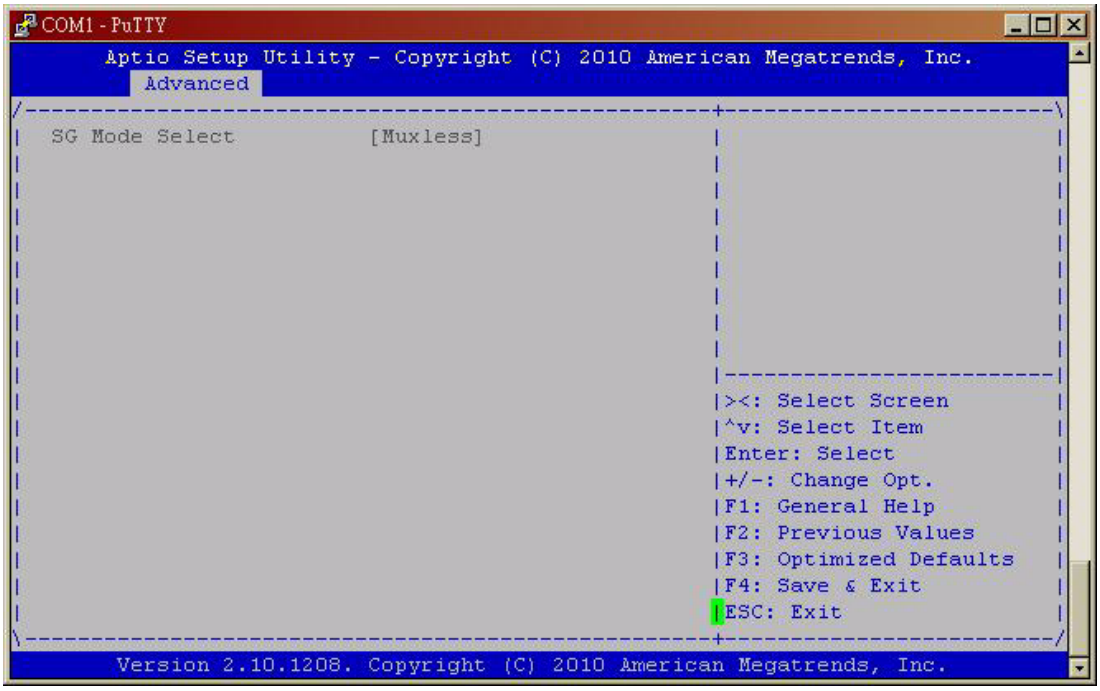


Figure 2.20 Switchable Graphics

- **SG Mode Select**
  This item allows users to select switchable graphics mode.

2.3.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI express Configuration, to go to the sub menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub menus are described on the following pages.

2.3.3.1 PCH-IO Configuration

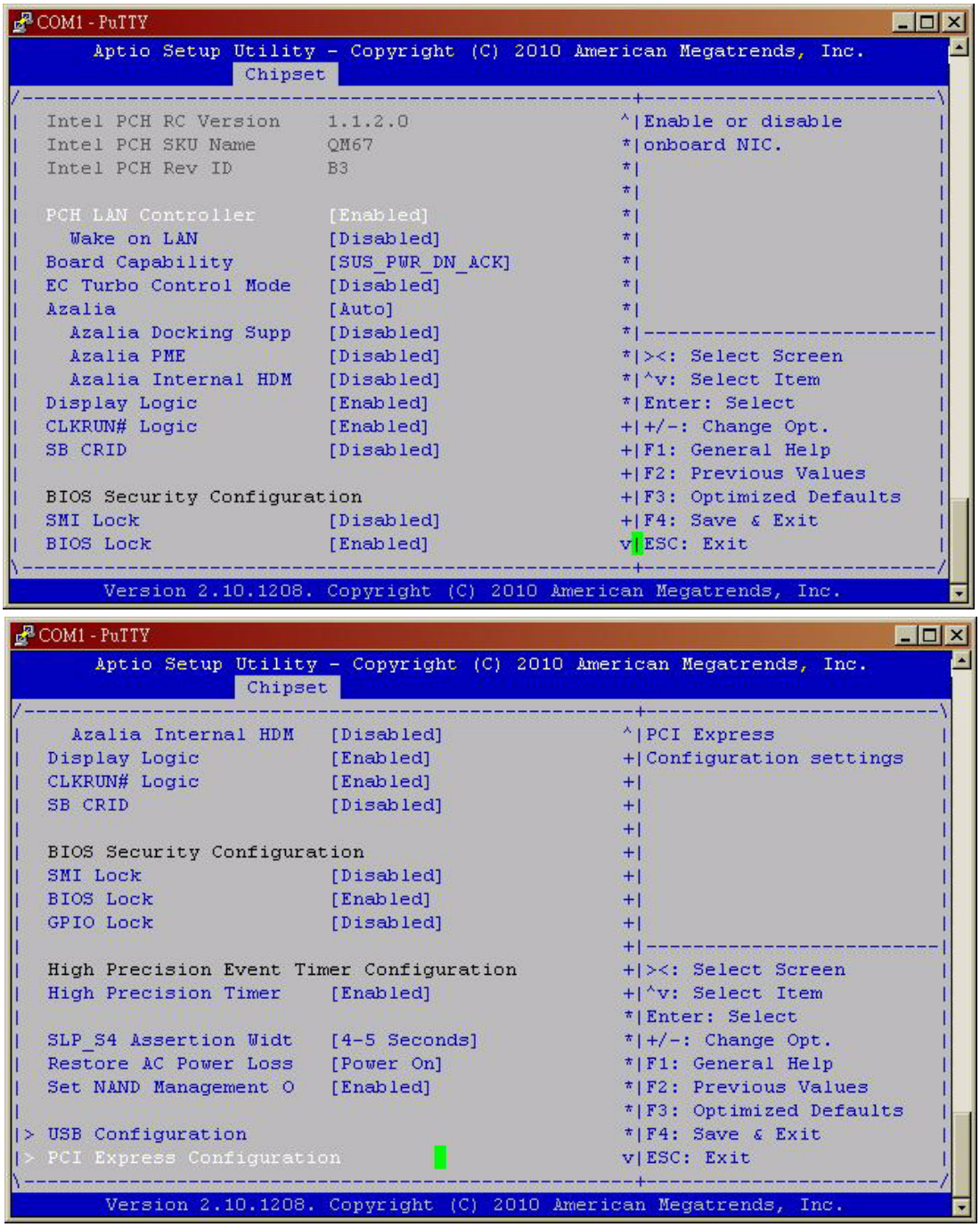


Figure 2.21 PCH-IO Configuration

- **PCH LAN Controller**
  Enable or disable PCH LAN controller.

- **Wake on LAN**
  Enable or disable PCH LAN wake up from sleep state.
- **Azalia Controller**
  Enable or disable the azalia controller.
- **Azalia Internal HDMI codec**
  Enable or disable the azalia internal HDMI codec.
- **High Precision Timer**
  Enable or disable the high precision timer.
- **SLP_S4 Assertion Width**
  This item allows users to set a delay of sorts.
- **Restore AC Power Loss**
  This item allows users to select off, on and last state.

2.3.3.2 North Bridge Configuration

- **System Agent (SA) Configuration**

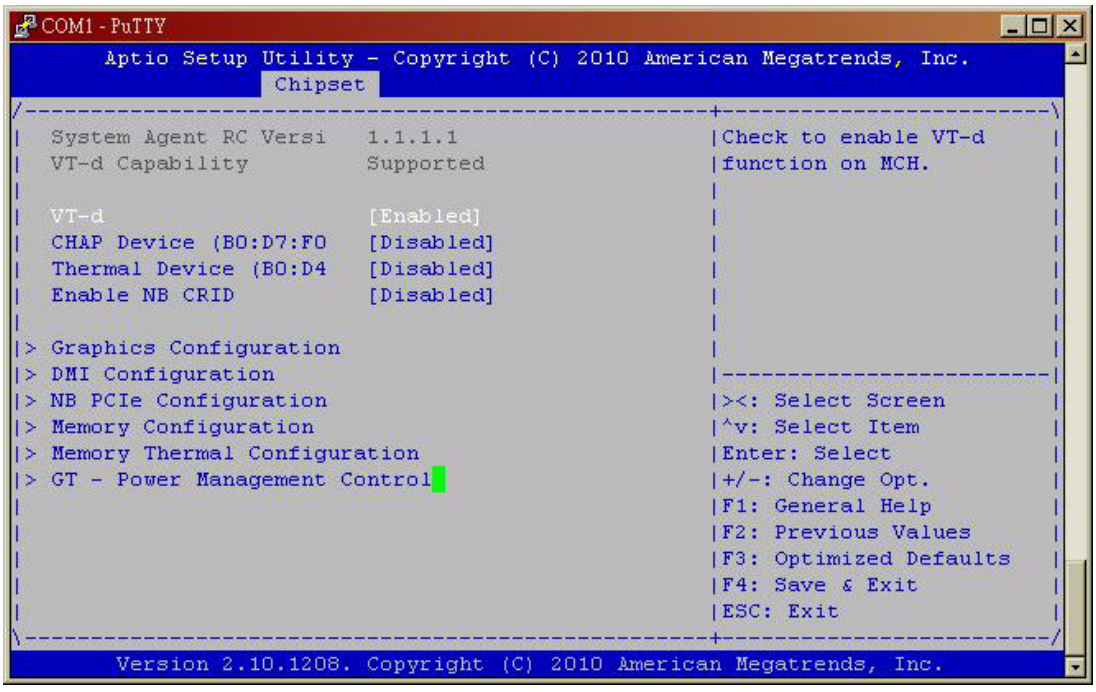


Figure 2.22 System Agent (SA) Configuration

  - **VT-d**
    This item allows users to enable or disable VT-d.

- **NB PCIe Configuration**

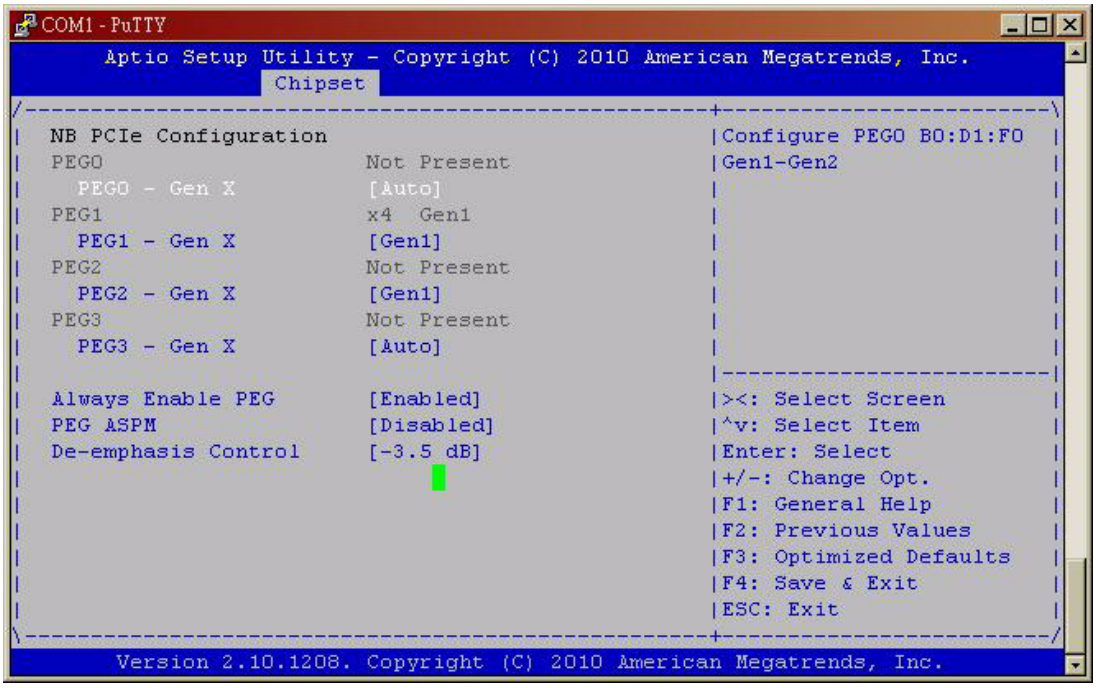


Figure 2.23 NB PCIe Configuration

- **PEG0 - Gen x**
  Select PEG0 speed.
- **Always enabled PEG**
  This item allows users to enable or disable PEG always.
- **PEG ASPM**
  This item allows users to enable or disable PEG ASPM.

Graphic Configuration

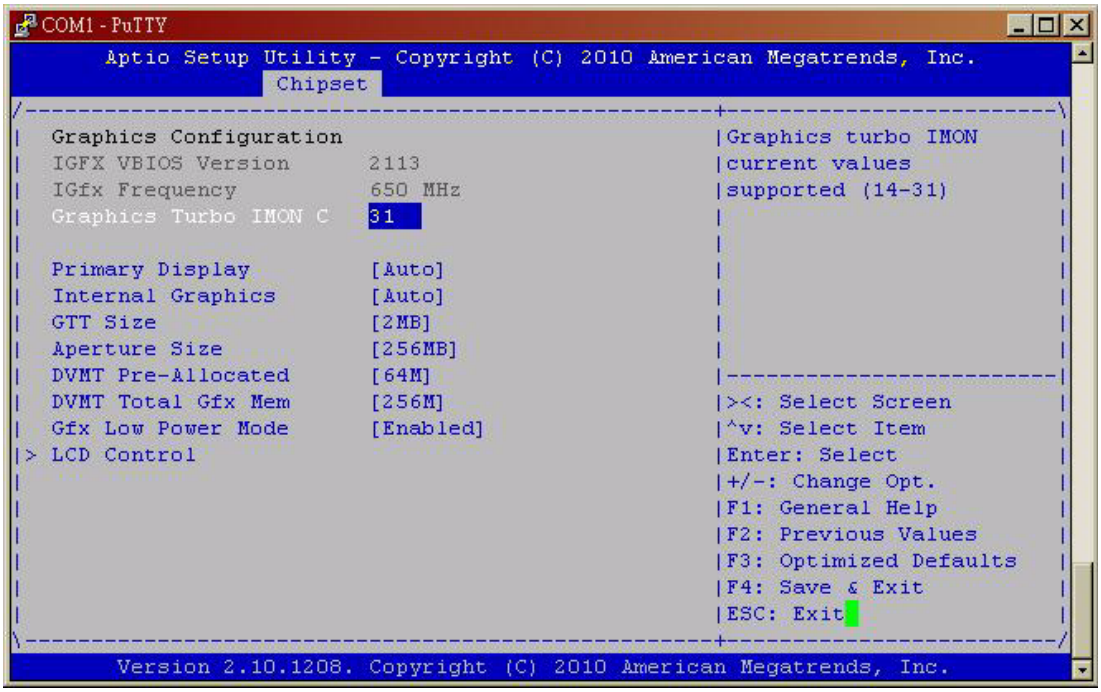


Figure 2.24 Graphic Configuration

– **Primary Display**

This item allows users to select which graphic controller to use as the primary boot device.

- **LCD Control**

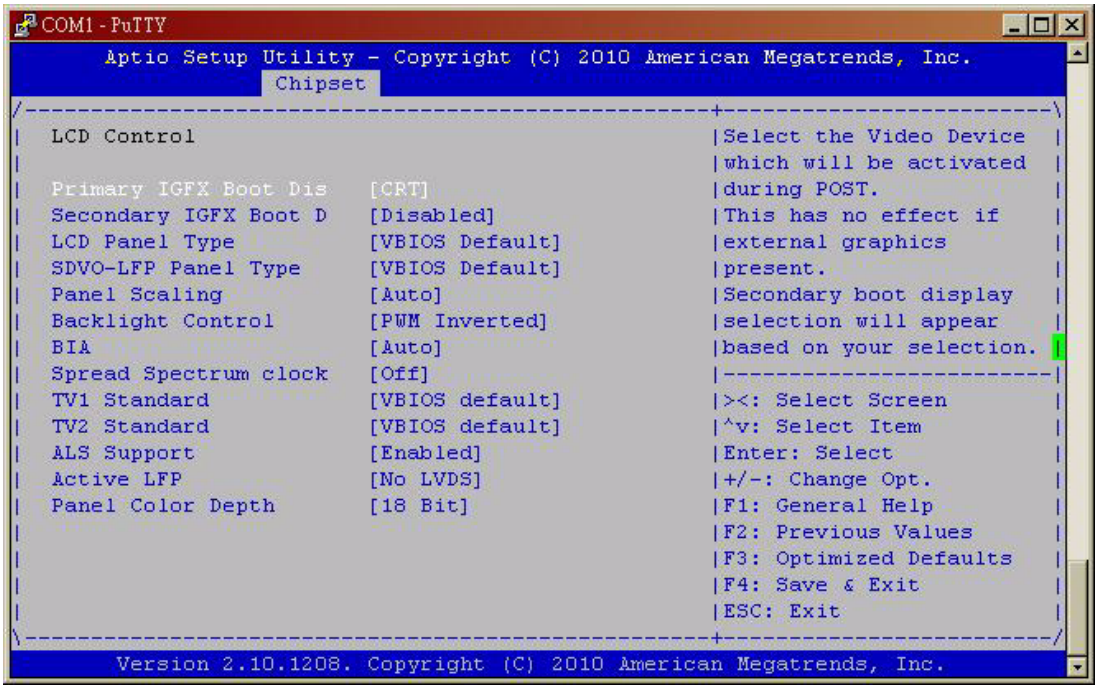


Figure 2.25 LCD Control

- **Primary IDFX Boot Display**
  Select boot display device at post stage.
- **LCD Panel Type**
  This item allows users to select panel resolution.
- **Panel Scaling**
  This item allows users to enable or disable panel scaling.
- **Active LFP**
  This item allows users to select LFP configuration.

2.3.3.3 PCI Express Ports Configuration

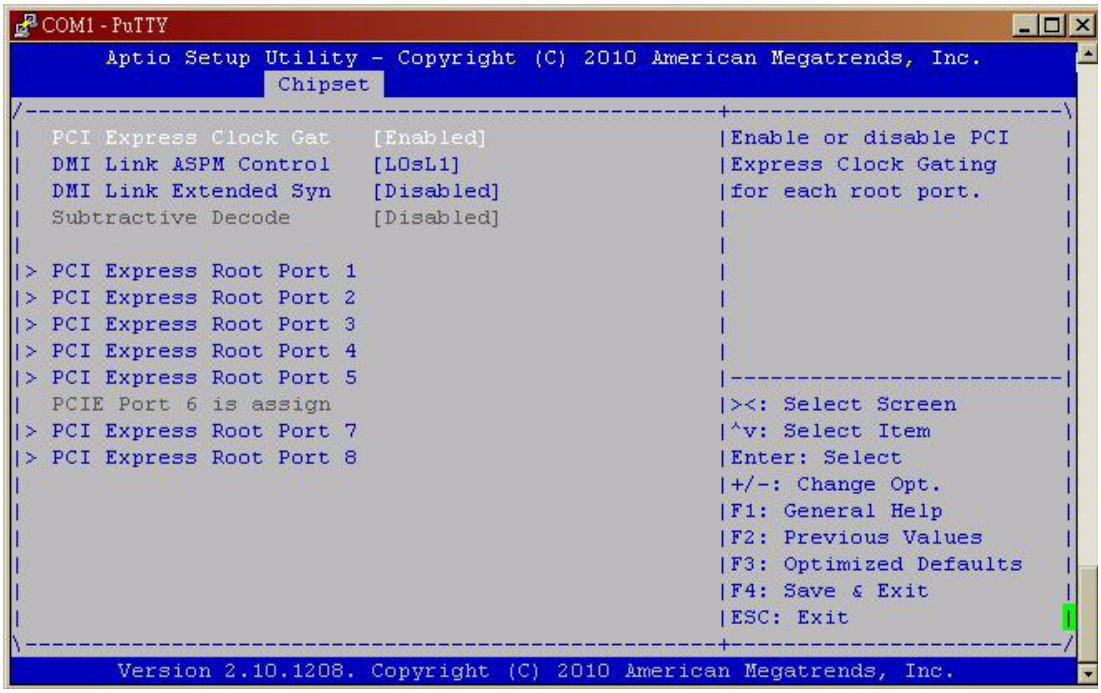
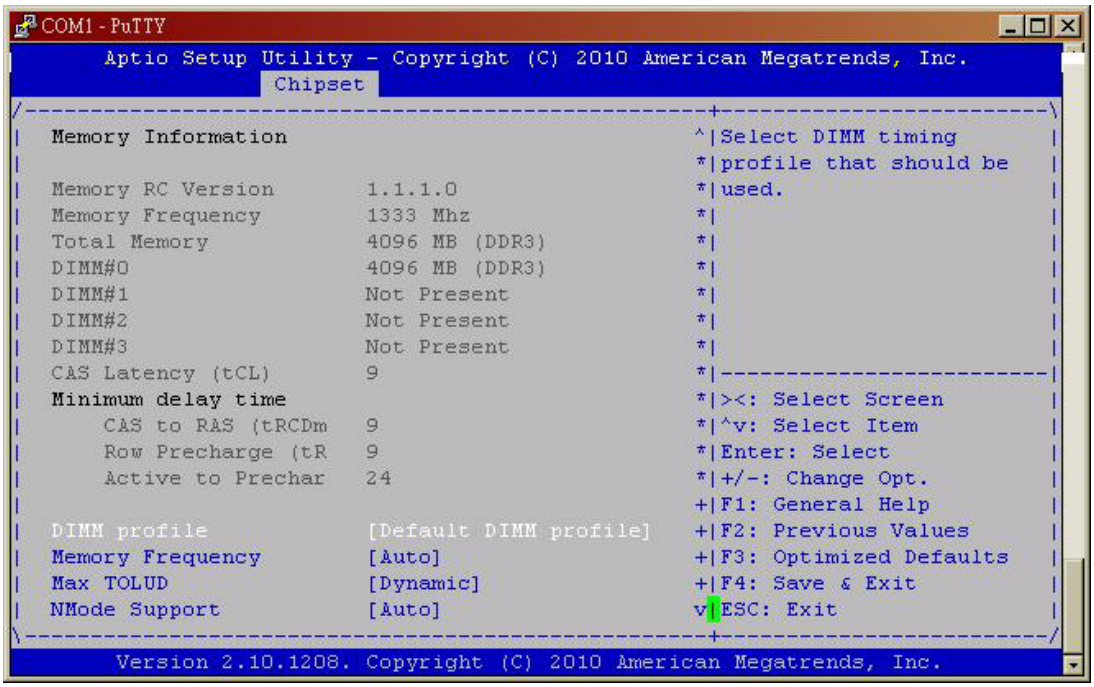


Figure 2.26 PCI Express Ports Configuration

Enable or disable PCI Express Clock Gating for each root port.

2.3.3.4 Memory Configuration



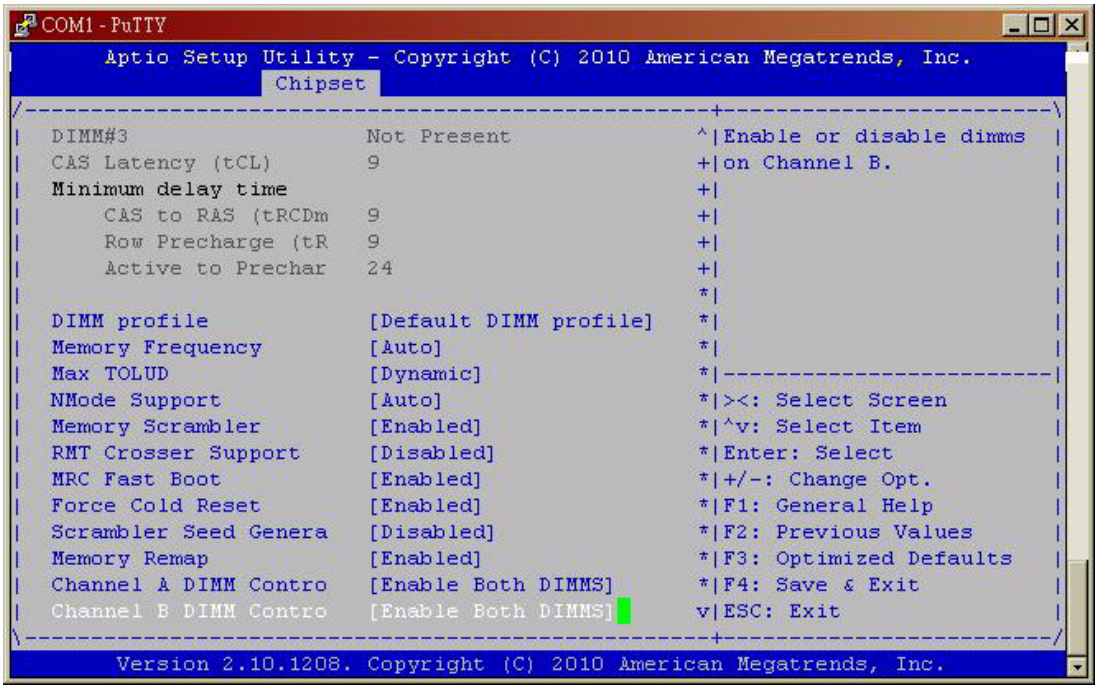


Figure 2.27 Memory Configuration

- **DIMM Profile**
  Select DIMM timing profile that should be used.
- **Channel A/B DIMM Control**
  Enable or disable DIMMs on channel A or B.

2.3.3.5 Memory Thermal Configuration

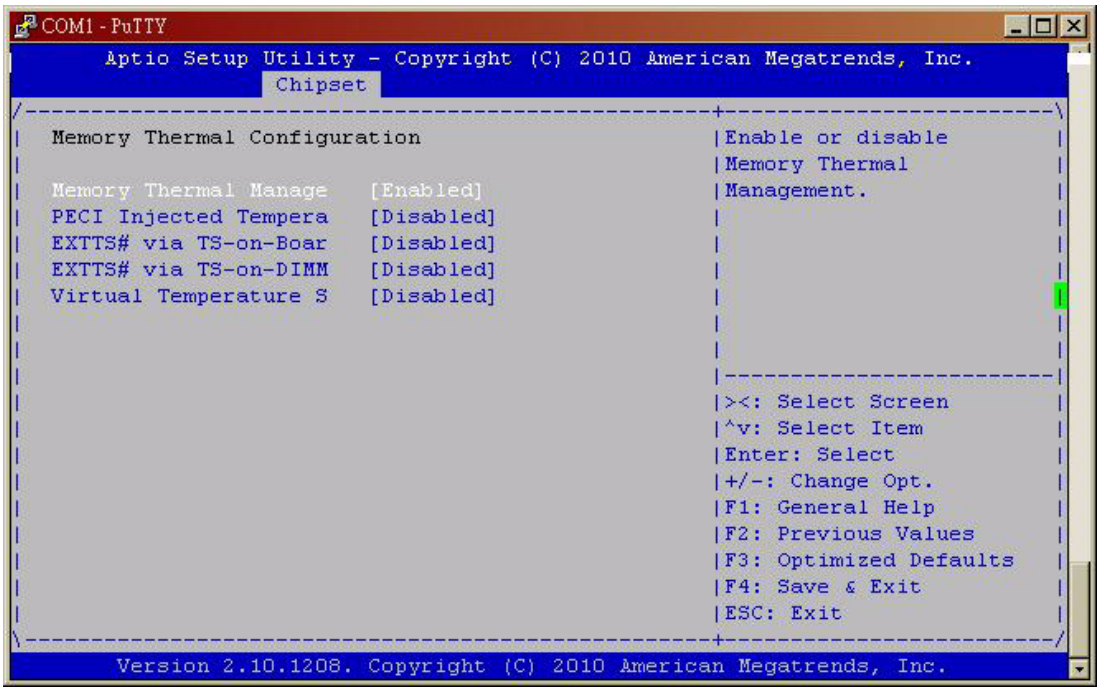


Figure 2.28 Memory Thermal Configuration

Enable or disable memory thermal management.

2.3.3.6 USB Configuration

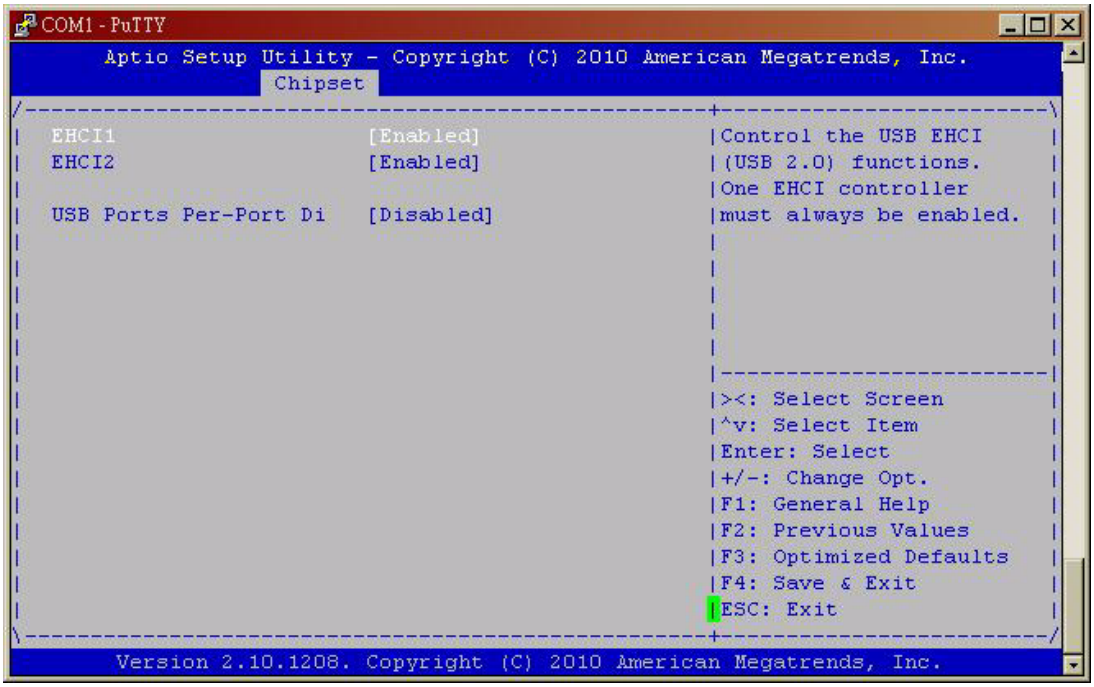


Figure 2.29 USB Configuration

Disable / Enable the USB controller (EHCI #1) and (EHCI #2) and allow users to disable/ enable USB ports.

2.3.4 Boot Setting

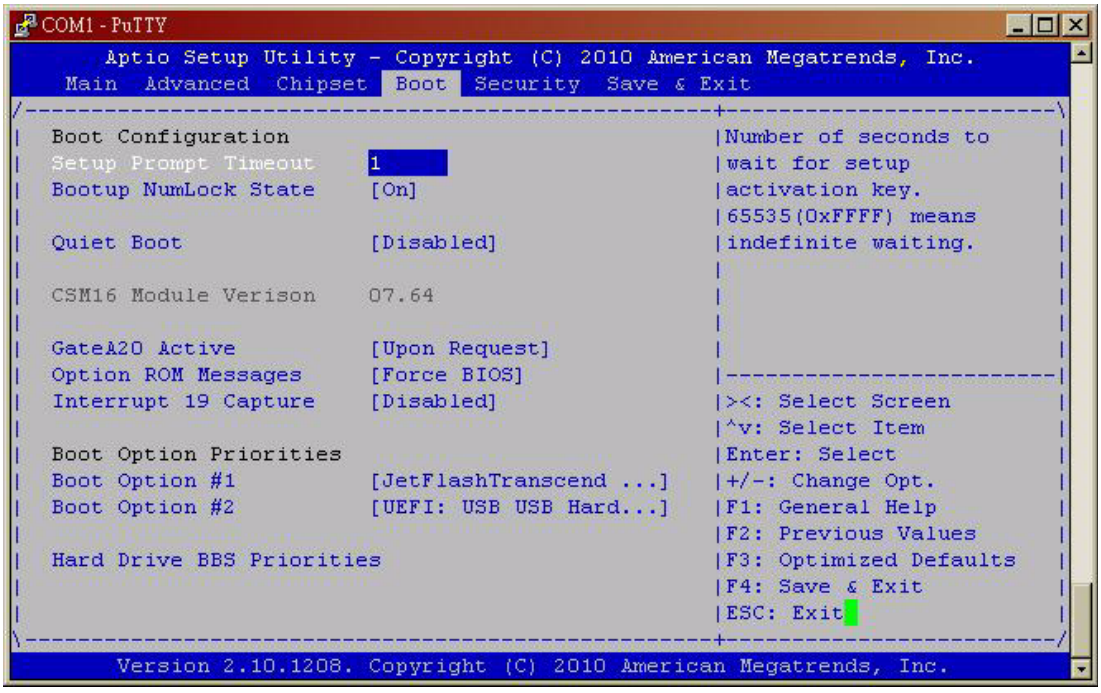


Figure 2.30 Boot Setting

2.3.4.1 Quiet Boot

If this option is set to Disabled, the BIOS displays normal POST messages. If enabled, an OEM Logo is shown instead of POST messages.

2.3.4.2 Fast Boot

This item allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.

2.3.4.3 Setup Prompt Timeout

Number of seconds waited for setup activation key. (65535 means indefinite wait.)

2.3.4.4 Bootup NumLock State

When "ON", the keyboard NumLock state will stay "ON" after boot. When "OFF", the keyboard NumLock state will stay "OFF" after boot.

2.3.4.5 Option ROM Message

Set display mode for Option ROM.

2.3.4.6 GateA20 Active

UPON REQUEST: GA20 can be disabled using BIOS services.

Always: do not allow disabled GA20.

2.3.4.7 Interrupt19 Capture

Enable/disable option for ROM to trap into 19.

2.3.4.8 Boot Option Priority

Boot Option #1

Boot Option #2

Show the boot device choices.

2.3.4.9 Hard Drive BBS Priorities

Select the main hard disk device type to be a boot hard drive.

2.3.5 Security Setting

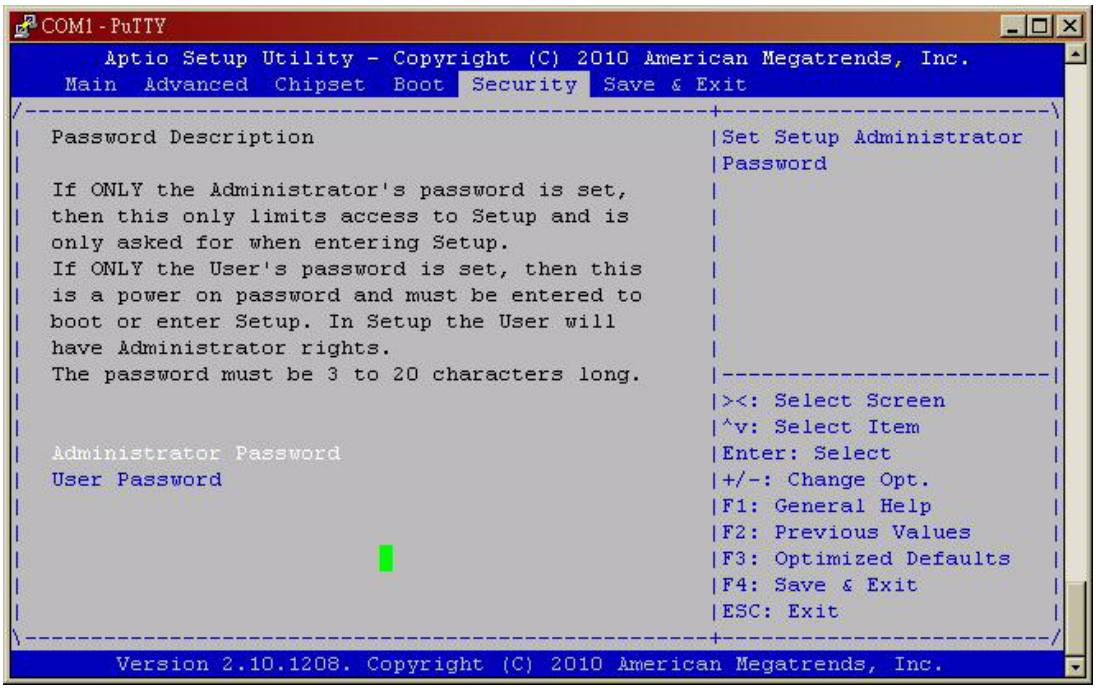


Figure 2.31 Security Setting

2.3.5.1 Administrator Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the Administrator password.

2.3.5.2 User Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the User Password.

2.3.6 PXE Boot Setting

2.3.6.1 Launch PXE OpROM

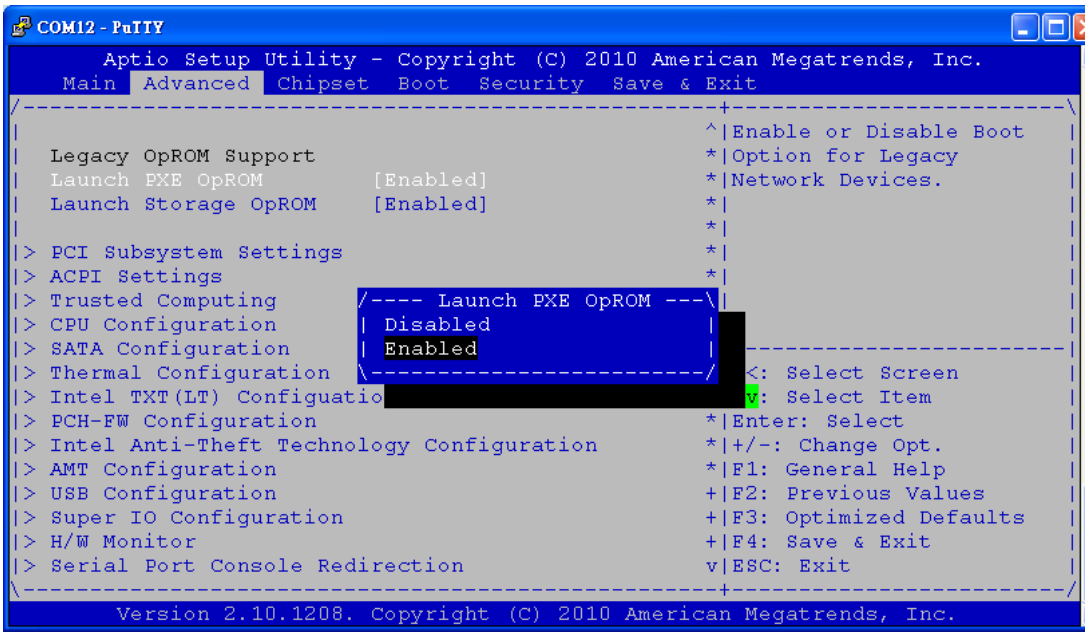


Figure 2.32 Launch PXE OpROM setting

Enable Launch PXE OpROM

2.3.6.2 Save Changes and Reset

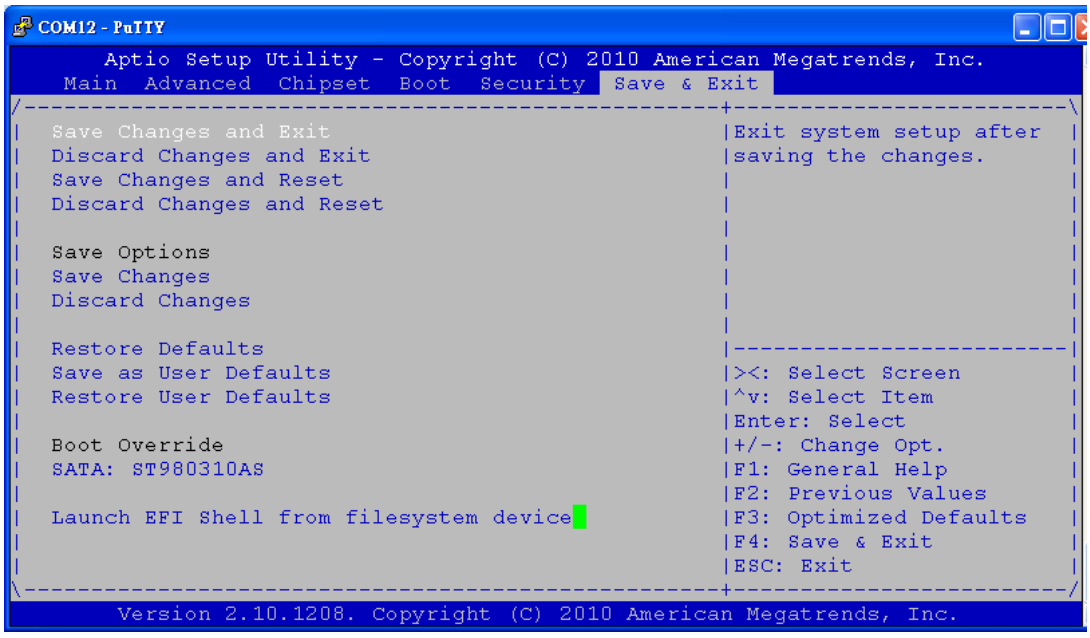
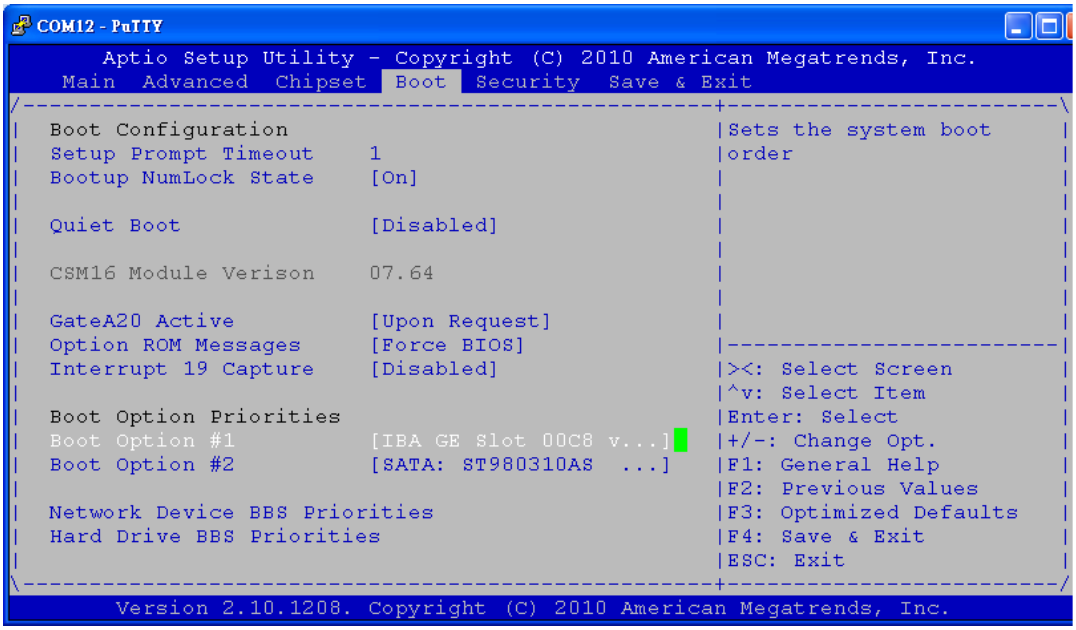
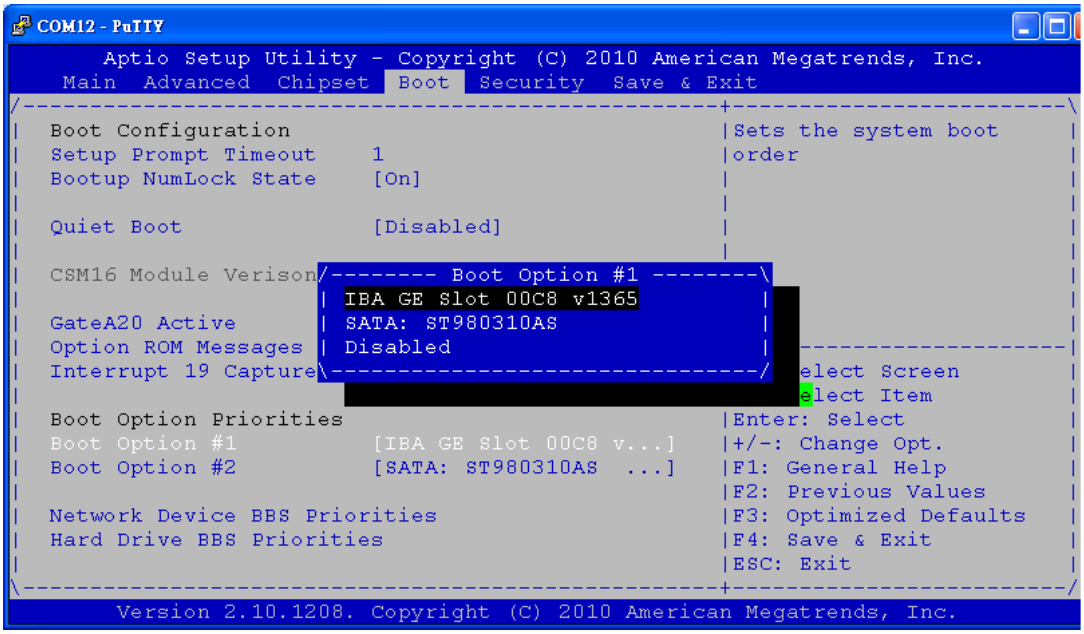
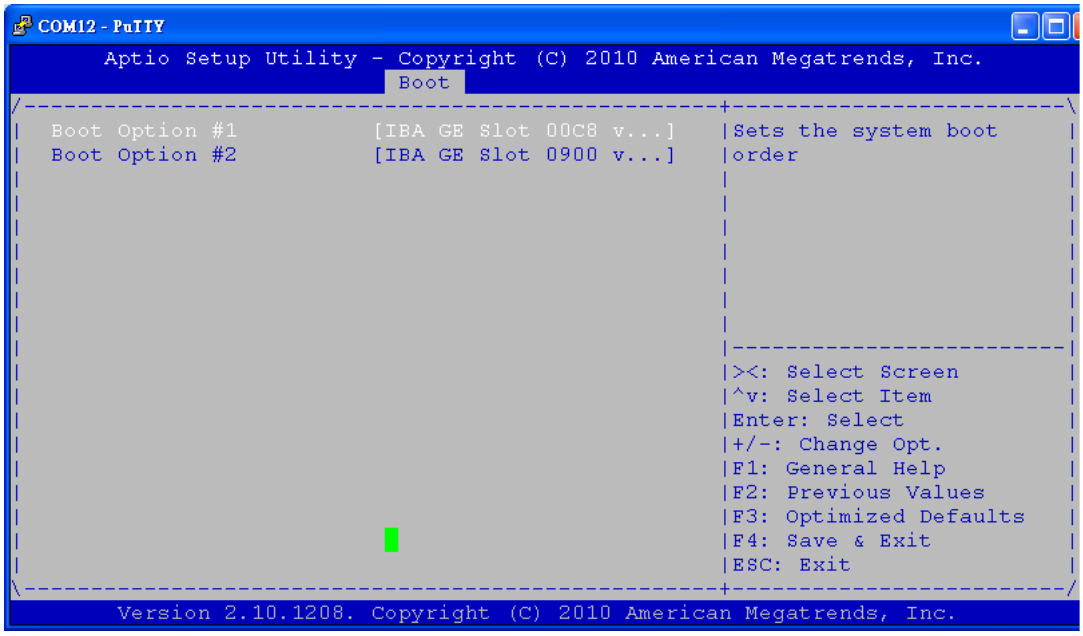


Figure 2.33 Save changes and reset

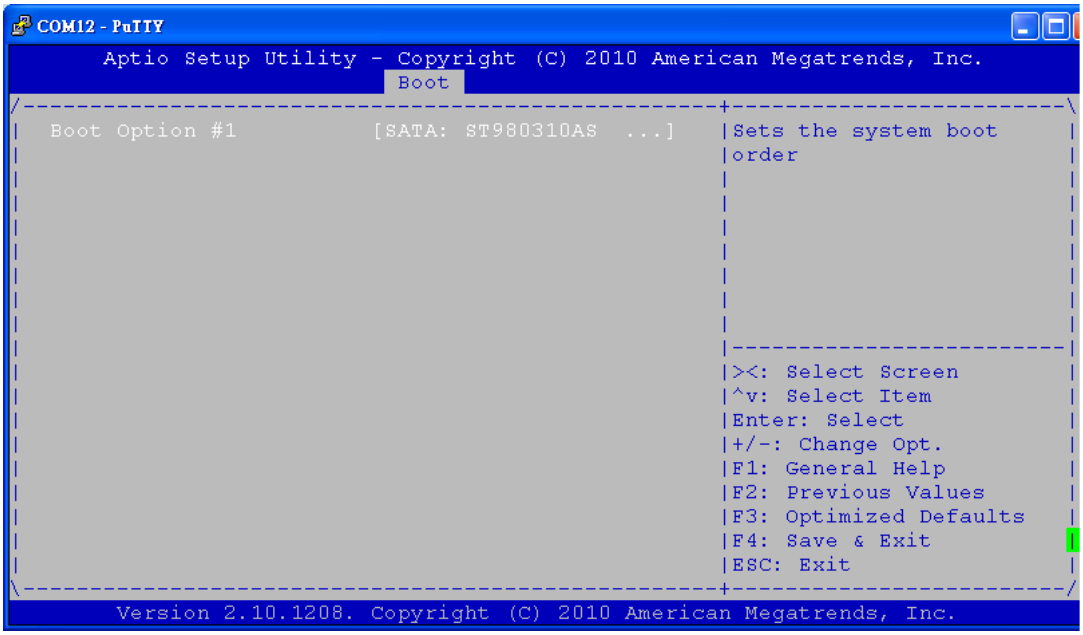
2.3.6.3 Choose boot option priority







Note 1: Network Device BBS Priorities



Note 2: Hard Drive BBS Priorities

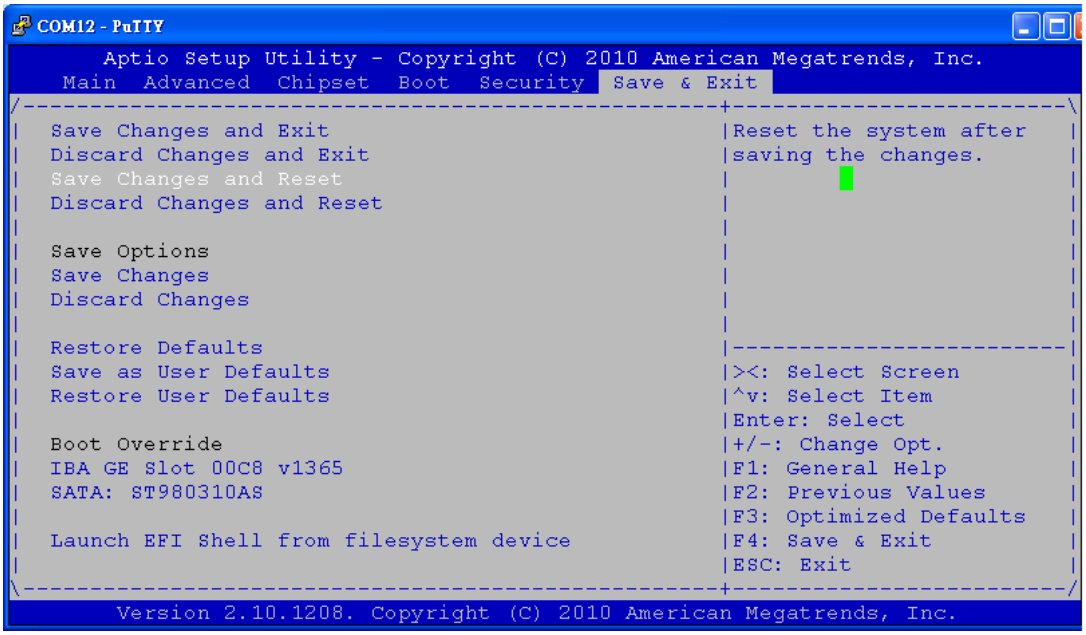


Figure 2.34 Boot option priority

2.3.6.4 Save Changes and Reset again

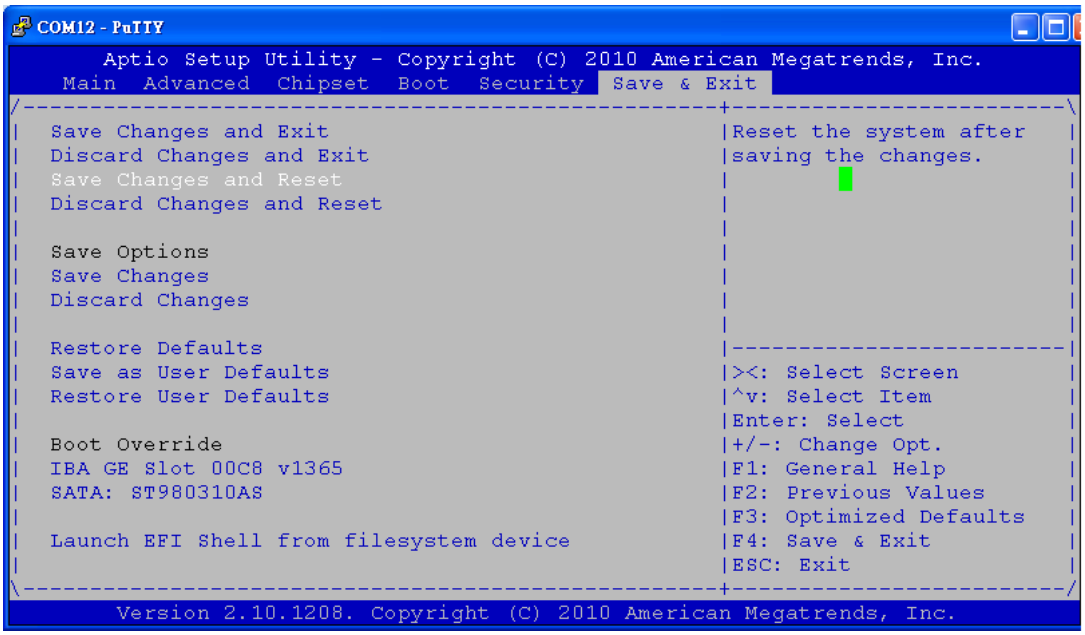


Figure 2.35 Save changes and reset

2.3.6.5 Start PXE Server

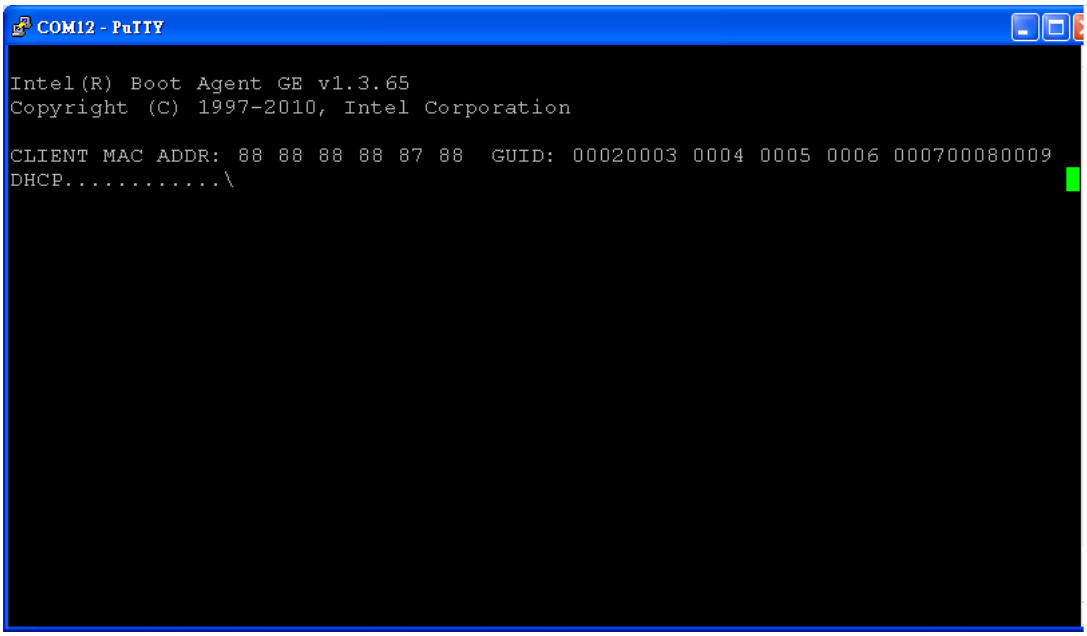


Figure 2.36 Start page of PXE Server

2.3.7 Save and Exit Configuration

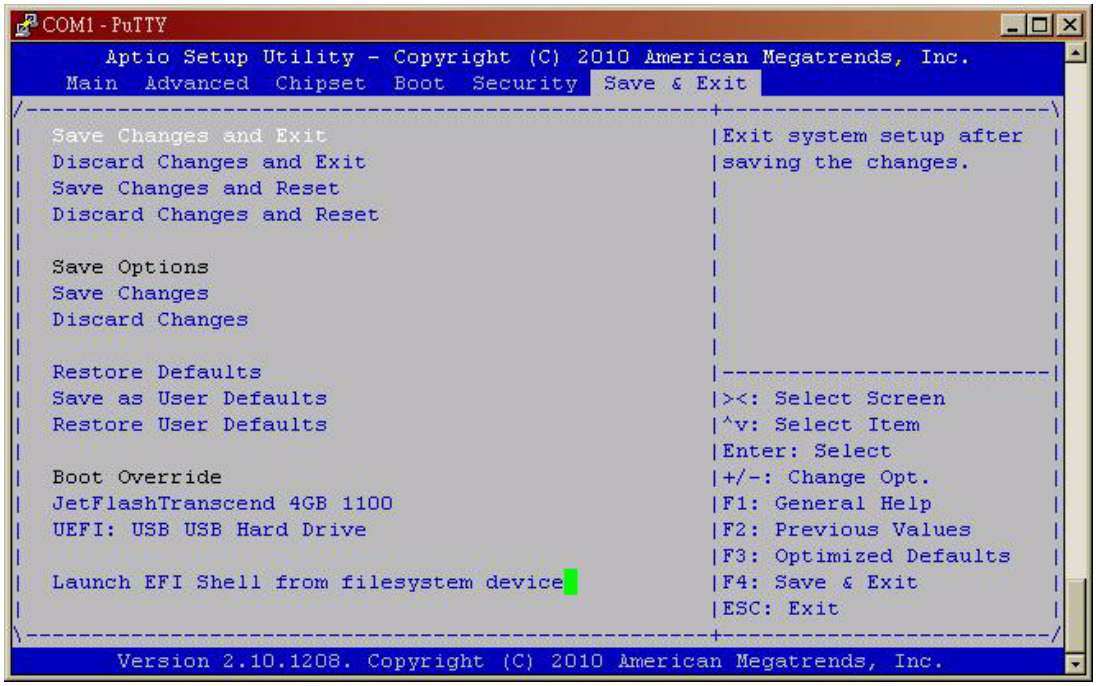


Figure 2.37 Save and Exit configuration

2.3.7.1 Save changes and Exit

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect all system configuration parameters.

1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
2. Select Ok or cancel.

2.3.7.2 Discard changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

1. Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
2. Select Ok to discard changes and exit. Discard Changes: Select Discard Changes from the Exit menu and press <Enter>.

2.3.7.3 Restore Defaults

The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

- **Save as User Default**

  Save the all current settings as user default.

- **Restore User Default**

  Restore all settings to user default values.

2.3.7.4 Boot Override

Show the boot device types on the system.

Chapter 3

IPMI for the MIC-3395

This chapter describes IPMI configuration for the MIC-3395.

3.1 Introduction

The MIC-3395 fully supports the IPMI 2.0 interface and the PICMG 2.9 R1.0 specification. The Renesas H8S/2167 has been implemented as the IPMI controller / Baseboard Management Controller (BMC) to run firmware and collect information. The MIC-3395 IPMI firmware is sourced from Avocent, a provider of proven and tested IPMI implementations in a wide range of mission-critical applications. The BMC's key features and functions are listed below.

- Compliant with IPMI specification, revision 2.0
- Compliant with PICMG 2.9 specification
- Environment monitoring (temperature and voltage)
- Power/Reset control via IPMI chassis command
- Complete SEL, SDR and FRU functionality
- FRU data capacity: 2 KB
- Provides 4 messaging interfaces
- One serial port
- One LPC interface
- One IPMB channel
- One LAN channel messaging via sideband NIC for out-of-band management
- Four I2C buses (including IPMB and SMBus) and two optional others
- Firmware Hub flashing and updating over serial port
- One hardware monitor
- One interrupt input
- Sensors threshold configuration
- Complete IPMI watchdog functionality (reset, power down, power cycle)
- Platform even filtering (PEF) and alert policies
- External Event Generation

3.2 Definitions

- **BMC - (Baseboard Management Controller):** This is the common abbreviation for an IPMI Baseboard Management Controller.
- **IPMB - (Intelligent Platform Management Bus):** A protocol defined for passing IPMI messages over a public I2C bus.
- **IPMI - (Intelligent Platform Management Interface):** A standardized system management interface. Please refer to the IPMI Specification for more details.
- **IPMIv2.0:** Specifically version 2.0 of IPMI

3.3 IPMI Function List

The following standard IPMI commands are supported.

Note!

The Network function (NetFn) field identifies the functional class of the message. The Network Function clusters IPMI commands into different sets. Please refer to the IPMI specification of network function codes for more information.

These command codes are compliant with the IPMI specification. Mandatory and Optional commands are defined in the IPMI specification.

For more details, please refer to the IPMI specification.

3.3.1 IPMI Device Global Commands

Table 3.1: Supported IPMI Device Global Commands

IPMI Device Global Commands	NetFn	Cmd	Mandatory / Optional
Get Device Id	App	0x01	M
Cold Reset	App	0x02	O
Get Self Test Results	App	0x04	M
Manufacturing Test On	App	0x05	O
Set ACPI Power State	App	0x06	O
Get ACPI Power State	App	0x07	O

3.3.2 BMC Device and Messaging Interfaces

The BMC messaging interfaces comply with the Intelligent Platform Management Interface Specification, Version 2.0. The MIC-3395 provides 4 messaging interface channels.

- **LPC/KCS channel:** Connects the H8S/2167 to the system LPC bus. Firmware sets 1 host interface over LPC: KCS for SMS.
- **IPMB channel:** Connects IPMB devices or connects to the H8S/2167's I2C_0 interface.
- **Serial port:** The H8S/2167 supports one serial port for out-of-band management (OOB) as well as one serial port for firmware flash update. Serial Port 0 is selected for OOB serial port
- **LAN channel:** OOB management over LAN is accomplished by a sharing a NIC (LAN3). This messaging interface channel connects the H8S/2167's I2C interface to the NIC's SMBus interface.

Table 3.2: H8S I2C Bus Connection to NIC SMBus

	H8S/2167 Pin Name	I2C address	Pin Number	System Connection
I2C_1	SCL1	0xC6	48	NIC SMBus clock
	SDA1		47	NIC SMBus data

Table 3.3: BMC Device and Messaging Commands

BMC Device and Messaging Commands	NetFn	Cmd	Mandatory/Optional
Set BMC Global Enables	App	0x2e	M
Get BMC Global Enables	App	0x2f	M
Clear Message Flags	App	0x30	M
Get Message Flags	App	0x31	M
Enable Message Channel Receive	App	0x32	O
Get Message	App	0x33	M
Send Message	App	0x34	M
Read Event Message Buffer	App	0x35	O
Get System GUID	App	0x37	O
Set Channel Access	App	0x40	O
Get Channel Access	App	0x41	O
Get Channel Info	App	0x42	O

Table 3.3: BMC Device and Messaging Commands			
Set User Access	App	0x43	O
Get User Access	App	0x44	O
Set User Name	App	0x45	O
Get User Name	App	0x46	O
Set User Password	App	0x47	O
Master Write-Read	App	0x52	M

3.3.3 BMC Watchdog Timer Commands

Table 3.4: BMC Watchdog Timer Commands			
BMC Watchdog Timer Commands	**NetFn**	**Cmd**	**Mandatory/Optional**
Reset Watchdog Timer	App	0x22	M
Set Watchdog Timer	App	0x24	M
Get Watchdog Timer	App	0x25	M

3.3.4 Event Commands

Table 3.5: Event Commands			
Event Command	**NetFn**	**Cmd**	**Mandatory/Optional**
Set Event Receiver	S/E	0x00	M
Get Event Receiver	S/E	0x01	M

3.3.5 PEF and Alerting Commands

Table 3.6: PEF and Alerting Commands			
PEF and Alerting Command	**NetFn**	**Cmd**	**Mandatory/Optional**
Get PEF Capabilities	S/E	0x10	M
Arm PEF Postpone Timer	S/E	0x11	M
Get PEF Configuration Parameters	S/E	0x13	M
Set Last Processed Event ID	S/E	0x14	M
Get Last Processed Event ID	S/E	0x15	M

3.3.6 SEL Device Commands

Table 3.7: SEL Device Commands			
SEL Device Command	**NetFn**	**Cmd**	**Mandatory/Optional**
Get SEL Info	Storage	Storage 0x40	M
Reserve SEL	Storage	Storage 0x42	O
Get SEL Entry	Storage	Storage 0x43	M
Get SEL Time	Storage	Storage 0x48	M
Set SEL Time	Storage	Storage 0x49	M

3.3.7 SDR Device Commands

Table 3.8: SDR Device Commands

SDR Device Command	NetFn	Cmd	Mandatory/Optional
Get SDR Repository Info	Storage	0x20	M
Reserve SDR Repository	Storage	0x22	M
Get SDR	Storage	0x23	M
Get SDR Repository Time	Storage	0x28	M
Set SDR Repository Time	Storage	0x29	M
Run Initialization Agent	Storage	0x2c	O

3.3.8 FRU Data

The MIC-3395 supports the IPMI FRU function to store accessible multiple sets of non-volatile Field Replaceable Unit (FRU) information in FRU EEPROM. The FRU data includes information such as serial number, part number, model, and asset tag. FRU information is accessed using IPMI commands compliant to the IPMI 2.0 specification as below.

Table 3.9: FRU Device Commands

FRU Device Command	NetFn	Cmd	Mandatory/Optional
Get FRU Inventory Area Info	Storage	0x10	M
Read FRU Inventory Data	Storage	0x11	M
Write FRU Inventory Data	Storage	0x12	M

3.3.9 Sensor and Threshold Configuration

Sensor data record (SDR) repository will be stored in BMC's flash memory and cannot be changed.

Note! *UNC = Upper Non-Critical.*

UC = Upper Critical

UNR = Upper Non-Recoverable

LNC = Lower Non-Critical

LC = Lower Critical

LNR = Lower Non-Recoverable

Table 3.10: Sensors List

Sensor Name	Sensor Number	Sensor Type	Sensor Reading Type	Logged Assertions	Logged De-assertions
Power Unit Status	50h	09h	6Fh	00h - Power Off	00h - Power Off
				04h - AC Lost	
Watchdog	51h	23h	6Fh	00h – Timer Expired, status only	N/A
				01h - Hard Reset	
				02h - Power Down	
				03h - Power Cycle	
Power Failure	52h	C0h	6Fh	00h - Power Failure	00h - Power Failure
Thermal Trip	53h	07h	6Fh	01h- Thermal Trip	01h - Thermal Trip
SEL Full	64h	D0h	01h	07h - over 75% full	N/A
				09h - over 90% full	
				0Bh - 100% full	
NCT6776F VCore	10h	02h	01h	LC, UC	LC, UC
NCT6776F 1.5 V	11h	02h	01h	LC, UC	LC, UC
NCT6776F 3.3 V	12h	02h	01h	LC, UC	LC, UC
NCT6776F 12 V	13h	02h	01h	LC, UC	LC, UC
NCT6776F 1.8 V	14h	02h	01h	LC, UC	LC, UC
NCT6776F 5 V	15h	02h	01h	LC, UC	LC, UC
NCT6776F 3.3 VB	16h	02h	01h	LC, UC	LC, UC
System Temp	20h	01h	01h	UC, UNR	UC, UNR
CPU PECI Temp	21h	01h	01h	UC, UNR	UC, UNR

Note! *A chassis intruder sensor is not used on the MIC-3395 platform.*

Power failure sensor type "C0h" indicates a power failure event.

Apart from the following list of sensors, other sensors should be re-initialized when the system is powered on or reset.

- *VCC*
- *SEL Fullness*
- *System PWR monitor*
- *Watchdog*

Table 3.11: Threshold Values of Sensors

Sensor Number	Entity Instance	Nominal Reading	UNR	UC	UNC	LNR	LC	LNC	Positive-going	Negative-going
10h	01h	1.0 V	N/A	1.52 V	N/A	N/A	0.3 V	N/A	0x02	0x02
11h	01h	1.5 V	N/A	1.65 V	N/A	N/A	1.35 V	N/A	0x02	0x02
12h	01h	3.3 V	N/A	3.63 V	N/A	N/A	2.97 V	N/A	0x02	0x02
13h	01h	12 V	N/A	13.2 V	N/A	N/A	10.8 V	N/A	0x02	0x02
14h	01h	1.8 V	N/A	1.98 V	N/A	N/A	1.62 V	N/A	0x02	0x02
15h	01h	5 V	N/A	5.5 V	N/A	N/A	4.5 V	N/A	0x02	0x02
16h	01h	3.3 V	N/A	3.63 V	N/A	N/A	2.97 V	N/A	0x02	0x02
20h	01h	35 C	70 C	60 C	N/A	N/A	N/A	N/A	0x02	0x02
21h	01h	70 C	100 C	90 C	N/A	N/A	N/A	N/A	0x02	0x02

Table 3.12: Sensor Device Commands

Sensor Device Command	NetFn	Cmd	Mandatory / Optional
Set Sensor Hysteresis	S/E	0x24	O
Get Sensor Hysteresis	S/E	0x25	O
Set Sensor Threshold	S/E	0x26	O
Get Sensor Threshold	S/E	0x27	O
Set Sensor Event Enable	S/E	0x28	O
Get Sensor Event Enable	S/E	0x29	O
Re-arm Sensor Events	S/E	0x2a	O
Get Sensor Event Status	S/E	0x2b	O
Get Sensor Reading	S/E	0x2d	M

3.3.10 Serial/Modem Device Commands

Table 3.13: Serial modem Device Commands

Serial/Modem Device Command	NetFn	Cmd	Mandatory / Optional
Set Serial/Modem Configuration Parameters	Transport	0x10	M
Get Serial/Modem Configuration Parameters	Transport	0x11	M
Set Serial/Modem Mux	Transport	0x12	M

3.4 BMC Reset

The BMC can initiate a graceful shutdown of the MIC-3395 by issuing a short pulse (~500 ms) on the power button signal to the ACPI controller when commanded through its host, OOB, or IPMB channels. It can also initiate a graceful shutdown from a Graceful Shutdown Event from the CMM or a Handle OPEN event. An ACPI compliant OS will then perform a graceful shutdown and light the blue LED whereas a non-compliant OS will just shut down.

Note!

The Network function (NetFn) field identifies the functional class of the message. The Network Function clusters IPMI commands into different sets. Please refer to the IPMI specification of network function codes for more information.

These command codes are compliant with the IPMI specification.

Mandatory and Optional commands are defined in the IPMI specification.

For more details, please refer to the IPMI specification.

Appendix A

Pin Assignments

This appendix describes pin assignments.

A.1 J1 Connector

Table A.1: J1 CompactPCI I/O

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	PAD(1)	5V	V(I/O)	PAD(0)	ACK64#	GND
23	GND	3.3V	PAD(4)	PAD(3)	5V	PAD(2)	GND
22	GND	PAD(7)	GND	3.3V	PAD(6)	PAD(5)	GND
21	GND	3.3V	PAD(9)	PAD(8)	M66EN(3)	C/BE(0)#	GND
20	GND	PAD(12)	GND	V(I/O)	PAD(11)	PAD(10)	GND
19	GND	3.3V	PAD(15)	PAD(14)	GND	PAD(13)	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12-14				KEY AREA			
11	GND	PAD(18)	PAD(17)	PAD(16)	GND	C/BE(2)#	GND
10	GND	PAD(21)	GND	3.3V	PAD(20)	PAD(19)	GND
9	GND	C/BE(3)#	IDSEL	PAD(23)	GND	PAD(22)	GND
8	GND	PAD(26)	GND	V(I/O)	PAD(25)	PAD(24)	GND
7	GND	PAD(30)	PAD(29)	PAD(28)	GND	PAD(27)	GND
6	GND	REQ0#	PRESENT#	3.3V	CLK0	PAD(31)	GND
5	GND	NC	NC	PCI_RST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	12V	5V	GND
Pin	Z	A	B	C	D	E	F

Note! *NC: No Connection*

#: Active Low

A.2 J2 Connector

Table A.2: J2 CompactPCI I/O

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	NC	NC	NC	GND
20	GND	CLK5	NC	NC	GND	NC	GND
19	GND	NC	GND	SMB_SDA	SMB_SCL	SMB_ALERT	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	PRST	REQ6#	GNT6#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
15	GND	NC	GND	FAL#	REQ5#	GNT5#	GND
14	GND	PAD(35)	PAD(34)	PAD(33)	GND	PAD(32)	GND
13	GND	PAD(38)	GND	V(I/O)	PAD(37)	PAD(36)	GND
12	GND	PAD(42)	PAD(41)	PAD(40)	GND	PAD(39)	GND
11	GND	PAD(45)	GND	V(I/O)	PAD(44)	PAD(43)	GND
10	GND	PAD(49)	PAD(48)	PAD(47)	GND	PAD(46)	GND
9	GND	PAD(52)	GND	V(IO)	PAD(51)	PAD(50)	GND
8	GND	PAD(56)	PAD(55)	PAD(54)	GND	PAD(53)	GND
7	GND	PAD(59)	GND	V(IO)	PAD(58)	PAD(57)	GND
6	GND	PAD(63)	PAD(62)	PAD(61)	GND	PAD(60)	GND
5	GND	C/BE(5)#	GND/64EN#	V(I/O)	C/BE(4)#	PAR64	GND
4	GND	V(I/O)	NC	C/BE(7)#	GND	C/BE(6)#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#(2)	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Note! *NC: No Connection*

#: Active Low

A.3 J3 Connector

PCIe port only supports X4 link

Table A.3: J3 CompactPCI I/O (LAN2/LAN3, 2.16)

J3	F	A	B	C	D	E	Z
1	GND	GND	GND	VCC5	GND	GND	GND
2	GND	PCIE_TX12+	PCIE_RX12+	VCC5	PCIE_TX13+	PCIE_RX13+	GND
3	GND	PCIE_TX12-	PCIE_RX12-	VCC5	PCIE_TX13-	PCIE_RX13-	GND
4	GND	GND	GND	VCC5	GND	GND	GND
5	GND	PCIE_TX14+	PCIE_RX14+	PLTRST#	PCIE_TX15+	PCIE_RX15+	GND
6	GND	PCIE_TX14-	PCIE_RX14-	TAP_TMS	PCIE_TX15-	PCIE_RX15-	GND
7	GND	GND	GND	TAP_TCK	GND	GND	GND
8	GND	PCIE_CLK+	NC	TAP_TRST#	NC	NC	GND
9	GND	PCIE_CLK-	NC	TAP_TDI	NC	NC	GND
10	GND	GND	NC	TAP_TDO	NC	NC	GND
11	GND	GND	GND	VCC3	GND	GND	GND
12	GND	SATA4_TX+	SATA4_RX+	VCC3	SATA2_TX+	SATA2_RX+	GND
13	GND	SATA4_TX-	SATA4_RX-	VCC3	SATA2_TX-	SATA2_RX-	GND
14	GND	GND	GND	VCC3	GND	GND	GND
15	GND	MDIB1+	MDIB1-	GND	MDIB3+	MDIB3-	GND
16	GND	MDIB0+	MDIB0-	GND	MDIB2+	MDIB2-	GND
17	GND	MDIA1+	MDIA1-	GND	MDIA3+	MDIA3-	GND
18	GND	MDIA0+	MDIA0-	GND	MDIA2+	MDIA2-	GND
19	GND	NC	NC	SATA_LED#	NC	NC	GND

Note! *NC: No Connection*

#: Active Low

A.4 J4 Connector

Table A.4: J4 CompactPCI I/O Port

Pin	Z	A	B	C	D	E	F
1	GND	NC	LVDS0_CLK+	GND	DDI3_AUX+	USB8_VCC	GND
2	GND	NC	LVDS0_CLK-	GND	DDI3_AUX-	USBD8-	GND
3	GND	NC	GND	GND	NC	USBD8+	GND
4	GND	NC	LVDS0_D0+	GND	DDI3_PAIR0+	GND	GND
5	GND	NC	LVDS0_D0-	GND	DDI3_PAIR0-	USB3_VCC	GND
6	GND	NC	LVDS0_D1+	GND	DDI3_PAIR1+	USBD3-	GND
7	GND	NC	LVDS0_D1-	GND	DDI3_PAIR1-	USBD3+	GND
8	GND	NC	LVDS0_D2+	GND	DDI3_PAIR2+	GND	GND
9	GND	NC	LVDS0_D2-	GND	DDI3_PAIR2-	DDI3_DDC_CLK	GND
10	GND	NC	LVDS0_D3+	GND	DDI3_PAIR3+	DDI3_DDC_DAT	GND
11	GND	NC	LVDS0_D3-	GND	DDI3_PAIR3-	DDI3_HPD	GND
12-14							
15	GND	NC	LVDS1_CLK+	GND	AUDIO_GND	MIC_L	GND
16	GND	NC	LVDS1_CLK-	GND	NC	MIC_R	GND
17	GND	NC	GND	GND	LINE_JD	LINEIN_L	GND
18	GND	NC	LVDS1_D0+	GND	LINEOUT_L	LINEIN_R	GND
19	GND	NC	LVDS1_D0-	GND	LINEOUT_R	LOUT_L	GND
20	GND	NC	LVDS1_D1+	GND	AUDIO_GND	LOUT_R	GND
21	GND	NC	LVDS1_D1-	GND	DDI3_DVIPWR	ADDIO_GND	GND
22	GND	NC	LVDS1_D2+	GND	LVDS_DDC_CLK	LVDS_BKLTEN	GND
23	GND	NC	LVDS1_D2-	GND	LVDS_DDC_DAT	LVDS_BKLTCTL	GND
24	GND	J4_GPIO1	LVDS1_D3+	GND	VBAT	LCD_VDD	GND
25	GND	J4_GPIO2	LVDS1_D3-	GND	PRST#	LCD_VDD	GND

Note! *NC: No Connection*

#: Active Low

A.5 J5 Connector

Table A.5: J5 CompactPCI I/O Port

J5	F	A	B	C	D	E	Z
1	GND	RTM_MDIA0+	RTM_MDIA0-	GND	RTM_MDIA1+	RTM_MDIA1-	GND
2	GND	RTM_MDIA2+	RTM_MDIA2-	GND	RTM_MDIA3+	RTM_MDIA3-	GND
3	GND	RTM_MDIB0+	RTM_MDIB0-	GND	RTM_MDIB1+	RTM_MDIB1-	GND
4	GND	RTM_MDIB2+	RTM_MDIB2-	GND	RTM_MDIB3+	RTM_MDIB3-	GND
5	GND	NC	GND	DDI2_DVIPWR	NC	NC	GND
6	GND	DDI2_AUX+	GND	DDI2_DDC_DAT	USB5_PWR	USB4_PWR	GND
7	GND	DDI2_AUX-	GND	DDI2_DDC_CLK	USBD5+	USBD4+	GND
8	GND	DDI2_PAIR0+	GND	MSDAT	USBD5-	USBD4-	GND
9	GND	DDI2_PAIR0-	GND	MSCLK	GND	GND	GND
10	GND	DDI2_PAIR1+	GND	PS2PWR	USB6_PWR	VGA_DDC_DAT	GND
11	GND	DDI2_PAIR1-	GND	KBDAT	USBD6+	VGA_DDC_CLK	GND
12	GND	DDI2_PAIR2+	GND	KBCLK	USBD6-	VGA_PWR	GND
13	GND	DDI2_PAIR2-	GND	DDI2_HPD	GND	VGA_VSYNC	GND
14	GND	DDI2_PAIR3+	GND	2.16A_LINK1000#	USB7_PWR	VGA_HSYNC	GND
15	GND	DDI2_PAIR3-	GND	2.16A_LIN100#	USBD7+	VGA_RED	GND
16	GND	RTMA_LINK1000#	RTMB_LINK100#	2.16A_LINK-ACT#	USBD7-	VGA_GREEN	GND
17	GND	RTMA_LINK100#	RTMB_LINK1000#	2.16B_LINK100#	GND	VGA_BLUE	GND
18	GND	RTMA_LINK-ACT#	RTMB_LINK-ACT#	2.16B_LINK1000#	UART2_RTS	GND	GND
19	GND	COM1_RX#	COM1_CTS#	2.16B_LINK-ACT#	COM2_DCD#	COM2_TX#	GND
20	GND	COM1_TX#	COM1_DSR#	RTM_PRES#	COM2_RTS#	COM2_DTR#	GND
21	GND	COM1_RTS#	COM1_DTR#	UART2_TXD	COM2_CTS#	COM2_RI#	GND
22	GND	COM1_DCD#	COM1_RI#	UART2_RXD	COM2_DSR#	COM2_RX#	GND

Note! *NC: No Connection*

#: Active Low

A.6 Other Connector

Table A.6: CNSATA1 Daughter Board Connector			
1	GND	2	GND
3	SATA0_TX+	4	SATA1_TX+
5	SATA0_TX-	6	SATA1_TX-
7	GND	8	GND
9	SATA0_RX+	10	SATA1_RX+
11	SATA0_RX-	12	SATA1_RX-
13	GND	14	GND
15	GND	16	GND
17	VCC5	18	VCC3
19	VCC5	20	VCC3

Table A.7: J15(P15) XMC1 Connector

Pin	A	B	C	D	E	F
1	PETX_P0	PETX_N0	+3.3V	PETX_P1	PETX_N1	VPWR(+5V)
2	GND	GND	NC(JRST#)	GND	GND	PRST#
3	PETX_P2	PETX_N2	+3.3V	PETX_P3	PETX_N3	VPWR(+5V)
4	GND	GND	NC(JTCK)	GND	GND	NC(MRSTO#)
5	PETX_P4	PETX_N4	+3.3V	PETX_P5	PETX_N5	VPWR(+5V)
6	GND	GND	NC(JTMS)	GND	GND	+12V
7	PETX_P6	PETX_N6	+3.3V	PETX_P7	PETX_N7	VPWR(+5V)
8	GND	GND	NC(JTDI)	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR(+5V)
10	GND	GND	NC(JTDO)	GND	GND	GA0
11	PERX_P0	PERX_N0	NC(MBIST#)	PERX_P1	PERX_N1	VPWR(+5V)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERX_P2	PERX_N2	NC(+3.3V_AUX)	PERX_P3	PERX_N3	VPWR(+5V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PERX_P4	PERX_N4	NC	PERX_P5	PERX_N5	VPWR(+5V)
16	GND	GND	NC(MVMRO)	GND	GND	TBD_SCLK
17	PERX_P6	PERX_N6	NC	PERX_P7	PERX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100Mhz	CLK_100Mhz#	FPGAIO2	NC(WAKE#)	NC(ROOT#)	NC

Table A.8: VCN1 VGA Connector			
1	RED	9	GND

2	+5 V	10	HSYNC
3	GREEN	11	VCC_EXT
4	GND	12	VSYN
5	BLUE	13	GND
6	NC	14	DDC_CLK
7	NC	15	GND
8	DDC_DATA	16	NC

Table A.9: CNCOM1 (RJ45) Connector			
1	DCD#	6	DSR#
2	SIN	7	RTS#
3	SOUT	8	CTS#
4	DTR#		
5	GND		

Table A.10: CN3 & CN7 USB Port 1 & Port 2			
1	+5 V (fused)	1	+5 V (fused)
2	USBD0-	2	USBD1-
3	USBD0+	3	USBD1+
4	GND	4	GND

Table A.11: BT1 CMOS Battery			
1	BAT_VCC	2	GND

Table A.12: RJ1 LAN1 Connector			
1	LAN_MDI 0+	5	LAN_MDI 2-
2	LAN_MDI 0-	6	LAN_MDI 1-
3	LAN_MDI 1+	7	LAN_MDI 3+
4	LAN_MDI 2+	8	LAN_MDI 3-

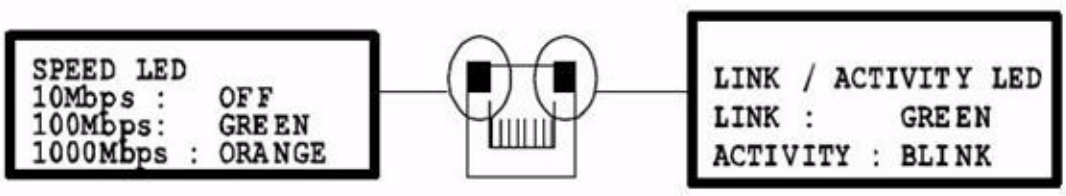


Figure A.1 RJ1 LAN1 Indicator

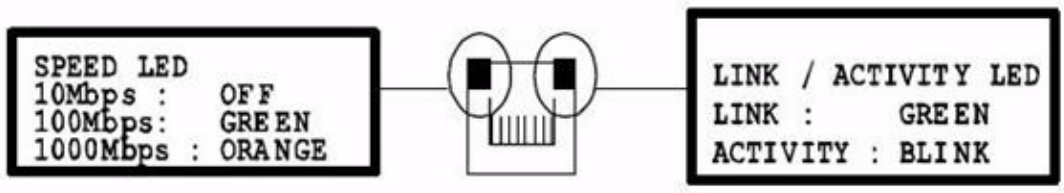
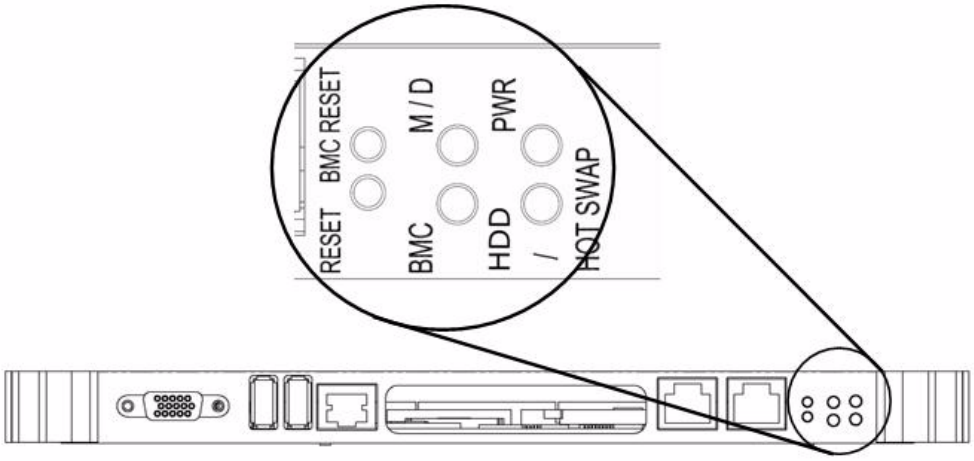


Figure A.2 RJ2 LAN2 Indicator

A.6.1 M/D, PWR, BMC HB, and IDE/Hot-swap LEDs



Name	Description
M/D (Green)	Indicates Master or Drone mode status
PWR (Green)	Indicates power status
BMC HB (Yellow)	Indicates BMC status (heart beat to indicate BMC active)
HDD/Hot Swap (Yellow/Blue)	Indicates IDE activity when yellow, or that the board is ready to be hot-swapped when blue.

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

B.1 Watchdog Timer Programming Procedure

To program the watchdog timer, you must execute a program that writes a value to I/O port address 443/444 (hex) for Enable/Disable. This output value represents time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is 1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
..	
3F	63 sec

After data entry, your program must refresh the watchdog timer by rewriting the I/O port 443 and 443 (hex) while simultaneously setting it. When you want to disable the watchdog timer, your program should read I/O port 444 (hex). The following example shows how you might program the watchdog timer in BASIC:

```
10 REM Watchdog timer example program
20 OUT &H443, data REM Start and restart the watchdog
30 GOSUB 1000 REM Your application task #1,
40 OUT &H443, data REM Reset the timer
50 GOSUB 2000 REM Your application task #2,
60 OUT &H443, data REM Reset the timer
70 X=INP (&H444) REM, Disable the watchdog timer
80 END
1000 REM Subroutine #1, your application task
.
1070 RETURN
2000 REM Subroutine #2, your application task
.
2090 RETURN
```

Appendix C

FPGA

This appendix describes FPGA configuration.

C.1 Features

- **Drone Mode**
- **Hot-Swap:** Hot insertion and removal control
- **CompactPCI Backplane:** CompactPCI slot Addressing
- **LPC Bus:** Provide LPC Bus access
- **Watchdog**
- **Debug Message:** Boot time POST message

C.2 FPGA I/O Registers

The Advantech MIC-3395 FPGA communicates with main I/O spaces. The LPC unit is used to interconnect the Intel ICH9R LPC signals. The Debug Port Unit is used to decode POST codes. The Hot-Swap Out-Of-Service LED Control Unit is used to control the blue LED during Hot-Insert and Hot-Remove. The Drone Mode Unit is used to disable the CPCI Bridge. The other signals in the Miscellaneous Unit are for interfacing with corresponding I/O interface signals.

Table C.1: LPC I/O Register Addresses

LPC Address	I/O Type	Description
0x 80h	W	Port 80 Display
0x 443h / 0x 444h	RW	Watchdog Register
0x 445h	R	FPGA revision
0x 447h	R	Geography Address (GA)

Appendix D

Glossary

D.1 Glossary

ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
CF	CompactFlash
CPU	Central Processing Unit
CPCI	CompactPCI
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EDMA	Enhanced DMA
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
FCBGA	Flip Chip BGA
FSB	Front Side Bus
HDD	Hard Disk Drive
HW	HardWare
I/O	Input/Output
IC	Integrated Circuit
IMCH	Integrated Memory Controller Hub
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
MAC	Medium Access Control
OS	Operating System
PCB	Printed Wiring Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical layer Interface
RASUM	Reliability, Availability, Serviceability, Usability and Manageability
RIO	Rear Input/Output
RS-232	An Interface specified by Electronic Industries Alliance
RTC	Real Time Clock
RTM	Rear Transition Module
SBC	Single Board Computer
SDRAM	Synchronous DRAM
SFP	Small From-factor Pluggable
SPD	Serial Presence Detect
SW	SoftWare
ULV	Ultra Low Voltage
XTM	Extension Module

ADVANTECH

Enabling an Intelligent Planet

www.advantech.com

Please verify specifications before quoting. This guide is intended for reference purposes only.

All product specifications are subject to change without notice.