PCI-1742U
16-bit, 1MS/s High-Resolution Multifunction Card

PIN Assignment

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AI0   68   34   AI1
AI2   67   33   AI3
AI4   66   32   AI5
AI6   65   31   AI7
AI8   64   30   AI9
AI10  63   29   AI11
AI12  62   28   AI13
AI14  61   27   AI15
AGND  60   26   AGND
AI16  59   25   AI17
AI18  58   24   AI19
AI20  57   23   AI21
AI22  56   22   AI23
AI24  55   21   AI25
AI26  54   20   AI27
AI28  53   19   AI29
AI30  52   18   AI31
AI32  51   17   AI33
AI34  50   16   AI35
AI36  49   15   AI37
AI38  48   14   AI39
AI40  47   13   AI41
AI42  46   12   AI43
AI44  45   11   AI45
AI46  44   10   AI47
AGND  43    9   AGND
AI48  42    8   AI49
AI50  41    7   AI51
AI52  40    6   AI53
AI54  39    5   AI55
AI56  38    4   AI57
AI58  37    3   AI59
AI60  36    2   AI61
AI62  35    1   AI63
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Signal Name	Reference	Direction	Description
AI<0…15>	AIGND	Input	Analog Input Channels 0 through 15. Each channel pair, AI<i, i+1> (i = 0, 2, 4…14), can be configured as either two single-ended inputs or one differential input.
AIGND	-	-	Analog Input Ground. The three ground references (AIGND, AOGND, and DGND) are connected together.
AO0_REF AO1_REF	AOGND	Input	Analog Output Channel 0/1 External Reference.
AO0_OUT AO1_OUT	AOGND	Output	Analog Output Channels 0/1
AOGND	-	-	Analog Output Ground. The analog output voltages are referenced to these nodes. The three ground references (AIGND, AOGND, and DGND) are connected together.
DI<0..15>	DGND	Input	Digital Input channels.
DO<0..15>	DGND	Output	Digital Output channels.
DGND	-	-	Digital Ground. This pin supplies the reference for the digital channels at the I/O connector as well as the +5VDC supply. The three ground references (AIGND, AOGND, and DGND) are connected together.
CNT0_CLK	DGND	Input	Counter 0 Clock Input. The clock input of counter 0 can be either external or internal , as set by software.
CNT0_OUT	DGND	Output	Counter 0 Output.
CNT0_GATE	DGND	Input	Counter 0 Gate Control.
PACER_OUT	DGND	Output	Pacer Clock Output. This pin pulses once for each pacer clock when turned on. If A/D conversion is in the pacer trigger mode, users can use this signal as a synchronous signal for other applications.
TRG_GATE	DGND	Input	A/D External Trigger Gate. When TRG _GATE is connected to DGND, it will disable the external trigger signal to input.
EXT_TRG	DGND	Input	A/D External Trigger. This pin is external trigger signal input for the A/D conversion. A low-to-high edge triggers A/D conversion to start.
+12V	DGND	Output	+12 VDC Source.
+5V	DGND	Output	+5 VDC Source.