

User Manual



MIC-3325

3U CompactPCI Intel Atom Dual/ Single Core Processor Blade



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Part No. 200K332500 Printed in Taiwan Edition 1 June 2012

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Technical Support and Assistance

- 1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
- 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Warnings, Cautions and Notes



Warning! Warnings indicate conditions, which if not observed, can cause personal injury!





Caution! Cautions are included to help you avoid damaging hardware or losing data. e.g.



There is a danger of a new battery exploding if it is incorrectly installed.

Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.



Notes provide optional additional information.

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- MIC-3325 single board computer (CPU heatsink and MCH heatsink included) x1
- Driver and user manual (PDF file) CD-ROM disc x1
- Daughter board for SATA HDD, HDD tray (Assembled with SBC dual slot ver-sion) x 1
- Warranty certificate document x1
- Safety Warnings: CE, FCC class A

Safety Instructions

- 1. Read these safety instructions carefully.
- 2. Keep this User Manual for later reference.
- 3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
- 4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
- 5. Keep this equipment away from humidity.
- 6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
- 7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
- 8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
- 9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
- 10. All cautions and warnings on the equipment should be noted.
- 11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
- 12. Never pour any liquid into an opening. This may cause fire or electrical shock.
- 13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
- 14. If one of the following situations arises, get the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated into the equipment.
 - The equipment has been exposed to moisture.
 - The equipment does not work well, or you cannot get it to work according to the user's manual.
 - The equipment has been dropped and damaged.
 - The equipment has obvious signs of breakage.
- 15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
- 16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

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Hardware Configuration

This chapter describes how to configure MIC-3325 hardware.

1.1 Introduction

Advantech's MIC-3325 is a 3U CompactPCI dual/single core processor blade based on the Intel® Atom[™] D525/N455+ICH8M two-chip platform. It enables a higher performance with 2 cores and 4 threads of processing power, lower cost, and easier validation. The MIC-3325 fully utilizes the I/O features of the Intel® chipsets, including an integrated memory controller (IMC), integrated graphics processing unit (GPU) and integrated I/O (IIO) such as DMI. The low power of the Intel Atom® makes it possible to work with high extended temperature ranges. Breakthrough memory design puts 2GB SDRAM on board while keeping the speed at DDR3 800MT/s. The directed soldered CPU and memory provide less weight and a higher shock/vibration resistance than socket devices. With such kind of benefits, the MIC-3325 can be used in critical applications, such as military defense, transportation, traffic control, test and measurement (T&M) as well as critical data acquisition & control applications.

MIC-3325 uses the Intel's ICH8M as the PCH which provides extensive I/O support. The Integrated Gigabit Ethernet Controller can operate at multiple speeds (10/100/ 1000 Mb/s) and in either full duplex or half duplex mode. A flexible 8HP extension module design makes MIC-3325 offer variations and provides additional I/O connectivity to the customer. For more details about the connectivity, please contact Advantech representative.

Table 1.1: M	IC-3325 Variant	S		
Model number	MIC-3325D-S1E	MIC-3325N-S1E	MIC-3325D-D1E	MIC-3325N-D1E
Slot Width	Single Slot (4HP)	Single Slot (4HP)	Dual Slots (8HP)	Dual Slots (8HP)
2 nd Layer XTM	-	-	1	1
Storage	CF	CF	CF/SATA HDD	CF/SATA HDD

1.2 Specifications

1.2.1 CompactPCI Bus Interface

The MIC-3325 is compliant with PICMG 2.0 Rev. 3.0. It supports a 32-bit / 33 MHz PCI bus for up to 8 CompactPCI slots at 3.3 V or 5 V VIO. The MIC-3325 is hot-swap compliant (PICMG 2.1).

1.2.2 CPU

The MIC-3325 supports the 45 nm technology Intel® Atom[™] Processor D525 /N455 processors with clock frequencies up to 1.8 GHz. Supported processors are listed in the table below. Forced airflow cooling is required.

Intel CPU	•	F	CPU	5.41	Dealar	0	CPU	Board	Required
Model NO.	Cores	Freq.	Architecture	DIMI	Раскаде	Cache	TDP TI	TDP	Airflow
D525 (4HP)	2	1.8 GHz	45 nm	250 MB/s	FCBGA	1 MB	13 W	16.6 W	10 CFM
N455 (4HP)	1	1.66 GHz	45 nm	250 MB/s	FCBGA	512 KB	6.5 W	14.6 W	Fanless
D525 (8HP)	2	1.8 GHz	45 nm	250 MB/s	FCBGA	1 MB	13 W	19.6 W	20 CFM
N455 (8HP)	1	1.66 GHz	45 nm	250 MB/s	FCBGA	512 KB	6.5 W	17.6 W	10 CFM

1.2.3 **BIOS**

A 2-MByte SPI flash contain a board-specific BIOS (from AMI) designed to meet industrial and embedded system requirements.

1.2.4 Chipset

The mobile Intel I/O Controller Hub 8-M (ICH8M) provides excellent flexibility for developers of embedded applications by offering increased I/O bandwidth and lower power consumption, which max. TDP is 2.4 W. It delivers outstanding system performance through high bandwidth interfaces such as PCI Express, Serial ATA and USB 2.0.

1.2.5 Memory

The MIC-3325 has 2GB of on-board DDR3-800 SDRAM.

1.2.6 Ethernet

There are three I/O LAN ports on the MIC-3325, which are implemented using two Intel 82583V LAN controllers (LAN2 on front panel, LAN3 on rear I/O via J2) and the ICH8M integrated LAN MAC + Intel 82567LM PHY (LAN1) to provide 10/100/1000 Base-T Ethernet connectivity.

1.2.7 Storage Interface

The MIC-3325 supports three SATA channels and one CompactFlash. The SATA1 interface can be routed to an onboard 2.5" SATA hard disk drive on second layer of dual slot XTM. The SATA2 interfaces are routed to the RIO via the J2 connector.

1.2.8 Serial Interface

Four UARTs (serial ports) come from Super IO. Two serial interfaces are routed to the RTM via the J2 connector. The rest two are for second layer on dual slot option-A.

1.2.9 USB Port

Six USB 2.0 compliant ports are provided. Two of them are routed to front panel connectors; one is routed to second layer on XTM option-A (two USB could be designed on option-B). The other two are routed to the RIO panel through the J2 connector.

1.2.10 LEDs

Three LEDs are provided on the front panel as follows:

Table 1.2: LED Indicator for the MIC-3325				
LED	Color	Indicator		
Hot swap	Blue	The board could be safely removed		
Power	Green	Power is provided to the board		
חטח	Green	HDD is activity		
עעח	Blinking	HDD is accessed		

1.2.11 Watchdog Timer

An on-board watchdog timer provides system reset capabilities via software control. The programmable time interval is from 1 to 255 seconds.

1.2.12 Optional Rear I/O Modules

The MIC-3525-S1E is the optional RTM (also known as rear I/O module) for the MIC-3325. It offers a wide variety of I/O panel features, such as one RJ45 LAN ports, one VGA port, and two USB2.0 ports. It also comes with on-board features such as one SATA (SATA pin-header) and two COM ports (pin-headers).

Table 1.3: RIO	Confi	guration	IS		
RIO Model Number	Rear F	Panel		On-board Header/Sc	ocket/Connector
MIC 3525 S1E	LAN	VGA	USB	SATA	СОМ
WIC-3525-51E	1	1	2	1	2

1.2.13 Optional Extension Modules

The MIC-3325 second layer XTM is used for MIC-3325x-DxE dual-slot platform, to increase the I/O feature set such as COM, USB, PS/2, etc. The XTM pin assignment and connectivity is described in detail in the Appendix. For a customized extension module demand, please contact Advantech local representative.

Table 1.4: The Second Layer XTM(8HP) Configurations						
XTM Model Number IO Panel				On-board Header/Socket/Connector		
	COM	USB	PS/2	Audio	SATA HDD	
MIC-3325XTM-S1E	2	1	1	-	1	

1.2.14 Mechanical and Environmental Specifications

Operating temperature: 0 ~ 60° C (32 ~ 140° F)

Note!

The operating temperature range of the MIC-3325 depends on the installed processor and the airflow through the chassis.

- Storage Temperature: -40 ~ 85° C (-40 ~ 185° F)
- Humidity(operating): 95% @ 40° C (non-condensing)
- Humidity (Non-operating): 95% @ 60° C (non-condensing)
- Vibration(Random operating): 5 ~ 100 Hz, 1.06 Grms(without on-board 2.5" HDD)
- Vibration (Sine Non-operating): 5 ~ 500 Hz, 2 Grms(with on-board 2.5" HDD)
- Bump (Non-operating): 15 G, 6 ms (without on-board 2.5" SATA HDD)
- Shock (operating): 10 G each face operating three times
- Shock (non-operating): 30 G each face non-operating three times
- Board size:
 - 3U/1 slot width (4HP): 100 x 160 x 20 mm (3.9" x 6.3" x 0.8")
 - 3U/2 slot width (8HP): 100 x 160 x 40 mm (3.9" x 6.3" x 1.6")
- Net Weight:
 - 3U/1 slot width (4HP): 0.28 kg
 - 3U/2 slot width (8HP): 0.40 kg

1.2.15 Compact Mechanical Design

Both MIC-3325N and MIC-3325D series has a specially designed heat sink for the processor. MIC-3325N series is capable for fanless operation. However, forced air cooling in the chassis is still needed for operational stability and reliability to MIC-3325D series.

1.2.16 CompactPCI Bridge

The MIC-3325 uses a Pericom PCIe to PCI bridge as a gateway to an intelligent subsystem. The PI7C9X110 bridge offers the following features:

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1

- Compliant with PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a
- PME support
- 3.3 V PCI signaling with 5 V I/O tolerance
- Provides two level arbitration support for eight PCI Bus masters
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support

Please consult the PI7C9X110 data sheet for details.

1.2.17 I/O Connectivity

The MIC-3325 provides rich I/O choices like the following table:

Table 1.5: I/O Connectivity								
Model Number IO Panel On-board Header/Socket/Connector								
	VGA	LAN	USB	COM	PS/2	SATA HDD	COM	SATA
First Layer	1	2	2	-	-	-	-	-
Second Layer	-	0	1	2	1	1	-	-
RIO	1	1	2		-	-	2	1

1.2.18 Hardware Monitor

One Hardware Monitor is available to monitor critical hardware parameters. It is attached to the super I/O (SMSC_SCH3114-NU/ SCH3106) to monitor the CPU and system temperature and core voltage, +5 V information.

1.2.19 Super I/O

The MIC-3325 Super I/O device provides the following legacy PC devices:

- Two UART ports are connected to the XTM as COM1 and COM2 on front panel. Two UART ports are connected to RIO via J2 as two on board RS-232
- The PS2 (keyboard/mouse) is routed to the XTM as PS/2 IO on front panel.

1.2.20 RTC and Battery

The RTC module keeps the date and time. On the MIC-3325 model the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3 V, 210 mAh).

1.3 Functional Block Diagram



Figure 1.1 MIC-3325 functional block diagram

1.4 Jumpers and Switches

Table 1.5 and table 1.6 list the jumper and switch functions. Figure 1.2 illustrates the jumper and switch locations. Please read this section carefully before changing the jumper and switch settings on MIC-3325.

Table 1.6: MIC-3325 Jumper Descriptions				
Number	Function			
J3 (1-2)	Normal			
J3 (2-3)	Clear CMOS			
JP1 (1-2)	VGA output from front panel (default)			
JP1 (2-3)	VGA output from rear IO panel			
J4	Drone Mode			
SW2*	Reset			





1.5 Connector Definitions

Table 1.7 lists the function of each connector and Figure 1.3 and 1.4 illustrate each connector location.

Table 1.7: MIC	-3325 Connector Descriptions
Number	Function
CN1	BIOS Socket
CN11	Programming CPLD code
CN3	RJ45 LAN existing exclusive with CN4,CN5
CN4	RJ45 LAN (Reserved design) exclusive with CN3, CN5
CN5	RJ45 LAN (Reserved design) exclusive with CN3, CN4
CN6	VGA (DB-15)
CN7	COMPACT FLASH DISK
CN8	USB on CPU board
CN9	USB on CPU board
CN10	Hot swap connector
CNXTM1	XTM connector 8HP
J1	Primary CompactPCI bus
J2	Rear I/O transition



Figure 1.3 MIC-3325 4HP front panel ports, indicators and buttons



Figure 1.4 MIC-3325 8HP front panel ports, indicators and buttons



Figure 1.5 MIC-3325 8HP (option-A) side view





	COM2 settin	ig ∎∶key
Deana	SW3	SW4
(Default)	1 2 3 4 5 6	1 2 3 4 5 6
	SW3	SVV4
RS422	1 2 3 4 5 6	1 2 3 4 5 6
	SW3	SVV4
RS485		1 2 3 4 5 6

Figure 1.7 COM1 setting on XTM (8HP Option-A)



Figure 1.8 RIO panel ports

Table 1.8: MIC-3325 XTM8HP Option-A Connector Descriptions

Number	Function
CN1	PS/2
CN2	COM1
CN3	COM2
CN4	SATA HDD CONN
CN5	USB Type A
XTM1	XTM

Table 1.9: MIC-3325 Rear I/O Connector Descriptions			
Number	Function		
CN1	VGA (DB15)		
CN2	СОМ		
CN3	СОМ		
CN4	RJ45 (LAN)		
CN5	SATA Wafer		
CN7	USB Type A		
CN8	USB Type A		

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your CompactPCI chassis before you work on it. Don't touch any components on the CPU board or other boards while the CompactPCI chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installation Steps

The MIC-3325 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an anti-static workbench.

1.7.1 MIC-3325 Installation Steps



Figure 1.9 Assemble board and front panel

The MIC-3325 supports 2.5" SATA hard disk drive on XTM (8HP) second layer. The XTM board is assembled on the MIC-3325X-D1E.

1.7.2 MIC-3325 Upgrade from 4HP to 8HP Installation Steps

1. Remove two posts on front panel.



2. Remove two screws on the bottom side.



3. Remove two screws on battery holder.



4. Uninstall the H/S cable to remove the 4HP front panel.



5. Install the 8HP panel and fix the H/S cable.



6. Fix the M2.5*5L screw in blue circle.



7. Fix the M2.5*8L screw in blue circle.



8. Fix the two M2.5*8L screws in blue circle.



Chapter 1 Hardware Configuration

9. Install four posts with M2.5*5L screws on the bottom side.



10. Remove the post on XTM board.



11. Fix the XTM board on the 4HP motherboard.



12. Fix four M2.5*5L screws.



13. Fix six posts on front panel.

1.7.3 MIC-3325 Rear I/O Board Installation Steps

The MIC-3325 supports either rear I/O board. The following picture shows the installation of the rear I/O board.



Figure 1.10 Assemble of MIC-3525 (MIC-3325 RIO)

1.8 Battery Replacement

The Battery model number is CR2032M1S8-LF, a 3 V, 210 mAh battery. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact with your local Sales to check the availability.

PN:1750129010 - BATTERY 3V/210 mAh with WIRE ASS'Y CR2032M1S8-LF.

1.9 Software Support

Windows XP, Windows XP Embedded, Windows 7 and Red Hat Enterprise Linux 6.1 have been fully tested on the MIC-3325. Please contact your local sales representative for details on support for other operating systems.

MIC-3325 User Manual



AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for over a decade. This section describes the BIOS which has been specifically adapted to the MIC-3325. With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of the MIC-3325. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-3325 setup screens.

			BIOS SE	TUP UTILITY		
Main	Advanced	PCIPnP	Boot	Security	Ch	ipset Exit
System	Overview					Use [ENTER], [TAB] or [SHIFT-TAB] to
AMIBIO Versio	S n :08.00.1	5				select a field.
Build ID	Date:02/14/1 :3325V11	2 0				Use [+] or [-] to configure system Time.
Proces Intel(Speed Count	sor R) Atom(TM) :1800MHz :1	CPU D525	€ 1.806	iHz		
System Size	Memory :2039MB					← Select Screen ↑↓ Select Item +- Change Field
System	Time		[00: 0	0:11]		Tab Select Field
System	Date		[Tue	01/01/2002]		F1 General Help F10 Save and Exit ESC Exit
	v02.61 (C) Copyr igh	t 1985-2	2006, America	n Meg	ratrends, Inc.
	E i au cu		- 4			

Figure 2.1 Setup program initial screen

The BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed up CMOS so it retains the Setup information when the power is turned off.

2.2 Entering Setup

Turn on the computer, and there should be a POST (Power-On Self Test) screen that shows the BIOS supporting the CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that the CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press and you will immediately be allowed to enter Setup.

American Megatrends	
AMIBIOS(C)2006 American Megatrends, Inc. **** MIC-3325 BIOS V1.10 (02/14/2012) **** CPU : Intel(R) Atom(TM) CPU D525 @ 1.80GHz Speed : 1.80 GHz	
Press DEL to run Setup Press F11 for BBS POPUP Currently Memory Frequency is : 800 Mhz Initializing USB Controllers Done. 2029MB OK	
The Revision ID of CPLD is: :102 USB Device(s): 1 Keyboard, 1 Storage Device Auto-detecting USB Mass Storage Devices Device #01 : Y-E USB-FDU *FullSpeed* 01 USB mass storage devices found and configured.	
Checking NVRAM	AUGE

Figure 2.2 Press to run setup

2.2.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

Main Advanced PCIF	BIOS SI 'nP Boot	ETUP UTILITY Security	Chipset	Exit
System Overview AMIBIOS Version :08.00.15 Build Date:02/14/12 ID :3325V110			Use or seli Use con	[ENTER], [TAB] [SHIFT-TAB] to ect a field. [+] or [-] to figure system Time.
Processor Intel(R) Atom(TM) CPU D5 Speed :1800MHz Count :1	25 @ 1.800	GHz		
System Memory Size :2039MB System Time System Date	[00 :([Tue	90:11] 01/01/2002]	+ †↓ +- Tab F1 F10 ESC	Select Screen Select Item Change Field Select Field General Help Save and Exit Exit

Figure 2.3 Main setup screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured whilst options in blue can. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIC-3325 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

BIOS SETUP UTILITY	
Main <mark>Advanced</mark> PCIPnP Boot Security	Chipset Exit
Advanced Settings	Configure CPU.
 WARNING: Setting wrong values in below sections may cause system to malfunction. CPU Configuration IDE Configuration SuperIO Configuration Numerul bits Configuration 	
 Hardware Health Configuration ACPI Configuration AHCI Configuration APM Configuration 	
 Event Log Configuration USB Configuration Clock Concentor Configuration 	 Select Screen Select Item Enter Co to Sub Screen
CIUCK Generator Contriguration	F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American	n Megatrends, Inc.

Figure 2.4 Advanced BIOS Features setup screen

2.2.2.1 CPU Configuration

BIOS SETUP UTILITY Advanced	
Configure advanced CPU settings Module Version:3F.14	Disabled for WindowsXP
Manufacturer:Intel Intel(R) Atom(TM) CPU D525 @ 1.80GHz Frequency :1.80GHz FSB Speed :800MHz Cache L1 :48 KB Cache L2 :1024 KB Ratio Actual Value:9	
Max CPUID Value LimitDisabled]Execute-Disable Bit CapabilityEnabled]Hyper Threading TechnologyEnabled]Intel(R) C-STATE techEEnabled]Enhanced C-States[Enabled]	 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit

Figure 2.5 CPU configuration

Max CPUID Value Limit

This item allows you to limit CPUID maximum value.

Execute-Disable Bit Capability

This item allows you to enable or disable the No-Execution page protection technology. The default setting for this item is set to "Enabled".

Hyper Threading Technology

This item allows you to enable or disable Intel® Hyper Threading technology. The default setting is "Enabled".

Intel(R) C-STATE tech

This item allows the CPU to save more power under idle mode.

Enhanced C-States

CPU idle set to enhanced C-States, disabled by Intel® C-STATE tech item. The default setting is "Enabled".

2.2.2.2 IDE Configuration

Advanced	BIOS SETUP UTILITY	
IDE Configuration		Options
ATA/IDE Configuration Configure SATA as	[Enhanced] [IDE]	Disabled Enhanced
 Primary IDE Master Primary IDE Slave Secondary IDE Master Secondary IDE Slave Third IDE Master Third IDE Slave 	: [Not Detected] : [Not Detected] : [Not Detected] : [Not Detected] : [Not Detected] : [Not Detected]	
Hard Disk Write Protect	Disabled]	 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit
v02.61 (C) Copyrig	ht 1985-2006, American Me	gatrends, Inc.

Figure 2.6 IDE configuration

IDE Configuration

The default setting is "Enhanced". "Enhanced" enables all SATA resources.

Enhanced Mode

Two options are available: IDE and AHCI. The default setting is "IDE",Legacy IDE Mode Setting.

Primary/Secondary/Third/Fourth IDE Master and Slave

While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of four possible IDE devices.

- **Type:** Select the type of SATA driver.[Not Installed][Auto][CD/DVD][ARMD]
- LBA/Large Mode: Enables or Disables the LBA mode.
- Block (Multi-Sector Transfer) : Enables or disables data multi-sectors transfers.
- **PIO Mode:** Select the PIO mode.
- **DMA Mode:** Select the DMA mode.
- S.M.A.R.T. : Select the smart monitoring, analysis, and reporting technology.
- 32-Bit Data Transfer: Enables or disables 32-bit data transfer.

Hard Disk Write Protect

Disable or enable device write protection. Enable effectively only if device is accessed through BIOS. This option only functions under DOS. The default setting for this item is set to "Disabled".

2.2.2.3 Super I/O Configuration

Advanced	BIOS SETUP UTILITY	
Configure SCH3114 Super IO Ch Serial Port1 Address Serial Port2 Address Serial Port2 Address Serial Port3 Address Serial Port3 Address Serial Port4 Address Serial Port4 Address Serial Port4 IRQ	ipset [3F8] [4] [2F8] [3] [3E8] [11] [2E8] [10] [Disabled]	- Allows BIOS to Select Serial Port1 Base Addresses.
		 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit
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Figure 2.7 Super I/O configuration

Serial Port1/2/3/4 Address and IRQ

Used to select Serial Port1 / Serial Port2 /Serial Port3 /Serial Port4 base addresses and IRQ.

Auto Flow Control For Serial Port2

Two options are available: Enable and Disable. Setting 485 protocol for Serial port2.

2.2.2.4 Hardware Health Configuration

Advanced	BIOS SETUP UTILITY	
Hardware Health Configu	ration	Enables Hardware
H/W Health Function	[Enabled]	Device.
CPU Temperature :62 System Temperature :38	°C/143°F °C/100°F	
Vcore +3.3Vin +5Vin	:1.048 U :3.317 U : 4.896 U	
UBHI	: 3.048 V	 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit
υ02.61 (C) Cop	yright 1985-2006, Americ	an Megatrends, Inc.

Figure 2.8 Hardware health configuration

System temperature, CPU temperature and Voltage status can be checked on Hardware Health Configuration.

2.2.2.5 ACPI Configuration



Figure 2.9 ACPI Settings

Advanced ACPI Configuration

Use this section to configure additional ACPI options.

BIOS SETUP UT	ILITY
Havanced	
Advanced ACPI Configuration	Enable RSDP pointers
ACPI Version Features [ACPI v3.0] ACPI APIC support [Enabled]	 to 64-bit Fixed System Description Tables. Di ACPI version has some * Select Screen 14 Select Item *- Change Option F1 General Help F10 Save and Exit ESC Exit
u02.61 (C) Comunicati 1985-2006	Merican Megatrende The

Figure 2.10 Advanced ACPI configuration

ACPI version features

Enable RSDP pointers to 64-bit fixed system description tables. And set this value to allow or prevent the system to be complaint with the ACPI 1.0/2.0/3.0 specification.

ACPI APIC Support

Enable or disable ACPI APIC table pointer to RSDT pointer list. The default setting is "Enabled.

2.2.2.6 AHCI Configuration



Figure 2.11 AHCI configuration

AHCI Port0 /Port1 Detect

While entering setup, BIOS auto detects the presence of SATA devices. This displays the status of auto detection of SATA devices.

- Type : Select the type of devices connected to the system. [Not Installed][Auto]
- S.M.A.R.T. : Select the smart Self-monitoring, analysis, and reporting technology.

2.2.2.7 APM Configuration

BIOS SETUP UTILITY	
Advanced	
APM Configuration	Enable or disable
Power Management/APM [Enabled]	 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit
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Figure 2.12 APM configuration

APM Configuration

Two options are available. Enable and Disable. Default is Enable the Power Management function.

2.2.2.8 Event Log Configuration



Figure 2.13 Event log configuration

View Event log

You can View all unread events on the Event Log, those events log includes the errors and warnings through the BIOS boot up.

Mark all events as read

Mark all unread events log as read, then last option will be no log to viewed.

Clear Event log

Discard all unread events log as read, then first option will be no log to viewed.

2.2.2.9 USB Configuration

BIOS SETUP UTILITY		
Advanced		
USB Configuration	Enables support for	
Module Version - 2.24.3-13.4	option disables	
USB Devices Enabled : 1 Keyboard, 1 Drive	no USB devices are connected.	
Legacy USB Support [Enabled] Hotplug USB FDD Support [Auto]		
▶ USB Mass Storage Device Configuration		
	 Select Screen Select Item Change Option General Help Save and Exit ESC Exit 	
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Figure 2.14 USB configuration

Legacy USB Support

Enable support for legacy USB. Auto option disables legacy support if no USB device is connected. The default setting for this item is set to "Enabled".

Hotplug USB FDD Support

A dummy FDD device is created that will be associated with the hot plugged FDD later. Auto option creates this dummy device only if there is no USB FDD present.

USB Mass Storage Device Configuration

BIOS SETUP UTILITY Advanced	
USB Mass Storage Device Configuration USB Mass Storage Reset Delay [20 Sec] Device #1 Kingston DT Emulation Type [Auto] Device #2 USB Hotplug FDD Emulation Type [Auto]	Number of seconds POST waits for the USB mass storage device after start unit command.
	 Select Screen Select Item Change Option General Help Save and Exit ESC Exit
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Figure 2.15 USB mass storage device configuration

USB Mass Storage Reset Delay

Number of seconds POST waits for USB mass storage devices after start unit command.

USB Devices Emulation Type

Set the current USB Devices emulation type.[Auto][Floppy][Forced FDD][Hard Disk][CDROM].

If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

2.2.3 PCI/PnP Setup

Select the PCI/PnP tab from the MIC-3325 setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

BIOS SETUP UTILITY							
Main Advanced I	CIPnP Boot	Security Chips	et Exit				
Advanced PCI/PnP Sett	ings	N	D: lets the BIOS				
WARNING: Setting wron may cause s <u>u</u>	sections du on Y	evices in the system. ES: lets the perating system					
Plug & Play O/S	[No]	c	onfigure Plug and				
PCI Latency Timer	[64]	P	lay (PnP) devices not				
Palette Snooping	[Disabl	edl r	equired for boot if 👘				
PCI IDE BusMaster	[Enable	d] y a	our system has a Plug nd Play operating				
IRQ3	[Availa	blel s	ystem.				
IRQ4	[Availa	blel					
IRQ5	[Availa	blel 🗧 🗧	Select Screen				
IRQ7	[Availa	blel 🕴 🕇	↓ Select Item				
IRQ10	[Availa	blel +	- Change Option				
IRQ11	[Ava i la	blel F	1 General Help				
IRQ15	[Ava i la	blel F	10 Save and Exit				
		E	SC Exit				
	onumight 1985-200	6 Amorican Morat	ronde. Inc				
002.01 (0)(ohdi idur. 1202-500	ur nmer roall negat.					

Figure 2.16 PCI/PnP setup

Plug and Play O/S

Select "No" to let the BIOS configure all the devices in the system. Selecting "YES" will let the operating system configure Plug and Play (PnP) devices that are not required for boot if your system has a Plug and Play operating system. The default setting is "No".

PCI Latency Timer

This option sets the latency of all PCI devices on the PCI bus. The value in units of PCI clocks for PCI devices. The default setting is 64.

Palette Snooping

This item is designed to solve problems caused by some non-standard VGA card. When Enabled ,to informs the PCI devices that an ISA graphic device is installed, so the card will function correctly.

PCI IDE BusMaster

When set Enabled, BIOS uses PCI busmaster for Reading/Writing to IDE drivers. When set Disabled, BIOS uses PIO Mode to R/W IDE drivers.

IRQ3/4/5/7/10/11/15

When set to Available will specified IRQ is available to be used by PCI/PnP devices. When set to Reserved will specified IRQ will Reserved for use by legacy ISA devices.

2.2.4 Boot Setup



Figure 2.17 Boot setup

Note!					

"Hard Disk Drives" will only appear on the setup screen when at least a hard disk drive is connected to the MIC-3325.

2.2.4.1 Boot Settings Configuration

BIOS SETUP UTILITY Boot			
Boot Settings Configuration	Allows BIOS to skip certain tests while		
Quick BootLinabledlQuiet Boot[Disabled]Bootup Num-Lock[On]PS/2 Mouse Support[Auto]Wait For 'F1' If Error[Enabled]Hit 'DEL' Message Display[Enabled]Interrupt 19 Capture[Disabled]Bootsafe function[Disabled]	decrease the time needed to boot the system.		
	 Select Screen Select Item Change Option General Help Gave and Exit ESC Exit 		
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Figure 2.18 Boot settings configuration

Quick Boot

Allows BIOS to skip certain tests while booting. The system configure summary will be skipped. This will decrease the time needed to boot the system. The default setting is "Enabled".

Quiet Boot

Used to display OEM logo when the setting is "Enabled". The default setting, "Disabled", displays normal POST message.

Bootup Num-Lock

Select Power-on state for Numlock function.

PS/2 Mouse Support

Select support for PS/2 Mouse useful for DOS.

Wait For 'F1' If Error

Wait for the F1 key to be pressed if an error occurs.

Hit 'DEL' Message Display

Select display the message or not : Press DEL to run Setup in POST.

Interrupt 19 Capture

Allows option ROMs to trap interrupts 19. This is required by some PCI cards that provide a ROM based setup utility.

Bootsafe function

Select support the Bootsafe function or not.

Boot Device Priority

Specifies the Boot Device Priority sequence from available devices. [Hard Disk Device][Removable Device][CD-DVD ROM]

2.2.5 Security Setup



Figure 2.19 Password configuration

Select Security Setup from the MIC-3325 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

- Change Supervisor Password
- Change User Password

2.2.6 Advanced Chipset Settings

BIOS SETUP UTILITY	Test (
nain Havanced PCIPMP Boot Security Chi	ipset Exit						
Advanced Chipset Settings	Configure North Bridge						
WARNING: Setting wrong values in below sections may cause system to malfunction.							
 North Bridge Configuration South Bridge Configuration 							
	 ← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit 						
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Figure 2.20 Advanced chipset setting

2.2.6.1 North Bridge Chipset Configuration

BIOS SETUP UTILITY					
Chipset					
North Bridge Chipset Configuration	Options				
PCI MMIO Allocation: 46B To 3072MB Configure DRAM Timing by SPD [Enabled]	Enabled Disabled				
Initate Graphic Adapter [IGD] Internal Graphics Mode Select [Enabled, 8MB]	 ← Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit 				

Figure 2.21 North bridge chipset configuration

Configure DRAM Timing by SPD

Select the DRAM Timing by SPD or manually. This item allows you to enable or disable detect by DRAM SPD.

- Initate Graphic Adapter Select which graphic controller to use as the primary boot device. This item is not recommended to change.
- Internal Graphics Mode Select Select the amount of system memory used by the Internal graphics device.

2.2.6.2 South Bridge Chipset Configuration

BIOS SETUP UTILITY Chipset						
South Bridge Chipset Configura	Options					
USB Functions USB 2.0 Controller	[10 USB Ports] [Enabled]	Disabled 2 USB Ports				
LAN1 Intel 82567V Controller LAN1 Root Rom	[Enabled] [Disabled]	4 USB Ports 6 USB Ports				
LAN2 Boot Rom	[Disabled]	8 USB Ports				
		 ✓ Select Screen ↑↓ Select Item ← Change Option F1 General Help F10 Save and Exit ESC Exit 				
$\mu 02.61$ (C) Comminist	1985-2006 Amorican Mor	ratronde Inc				

Figure 2.22 South bridge chipset configuration

USB Functions

The default setting is "10 USB Ports".

USB 2.0 Controller

Enable and Disable the USB 2.0 Controller. When set 10 ports, it will be grayedout.

LAN1 Intel 82567V Controller Enable and Disable the Intel LAN1 Controller.

LAN1 Boot ROM Select heat from DCL DOM or Not 4

Select boot from PCI ROM or Not for LAN1.

LAN2 Boot ROM

Select boot from PCI ROM or Not for LAN2.

HDA Controller

Enable and Disable the HD audio Controller.

2.2.7 Exit Option

BIOS SETUP UTILITY							
Main	Advanced	PCIPnP	Boot	Security	Chi	pset Exit	
Exit (Dptions					Exit system setup	
Save (Changes and E	xit				changes.	
Discaı Discaı	rd Changes an rd Changes	d Exit				F10 keu can be used	
1		14-				for this operation.	
Load I Load I	Primal Defau Failsafe Defa	ults					
						 ← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit 	
	u02_61_0	C) Comurciad	+ 1985-20	006. America	. Men	atrends. Inc	

Figure 2.23 Exit options

2.2.7.1 Save Changes and Exit

When you have completed the system configuration changes, follow these steps:

- Select Exit Saving Changes from the Exit menu and press <Enter>. The following messages appear on the screen: Save Configuration Changes and Exit Now? [Ok] [Cancel]
- 2. Select "Ok" to save changes and exit.

2.2.7.2 Discard Changes and Exit

Follow these steps to quit Setup without making any permanent changes to the system configuration.

- Select Exit Discarding Changes from the Exit menu and press <Enter>. The following messages appear on the screen: Discard Changes and Exit Setup Now? [Ok] [Cancel]
- Select "Ok" to discard changes and exit. The following messages appear on the screen:
 Discard Changes
 - Discard Changes
- 3. Select "Discard Changes" from the Exit menu and press <Enter>.

2.2.7.3 Discard Changes

Discard changes done so far to any of the setup questions.

2.2.7.4 Load Optimal Defaults

This loads the optimal defaults values for the MIC-3325 which allows optimum functionality and system performance. Select "Load Optimal Defaults" from the Exit menu and press <Enter>.

2.2.7.5 Load Failsafe Defaults

This loads the basic defaults values for the MIC-3325 which may not work best for all computer applications. Select "Load Failsafe Defaults" from the Exit menu and press <Enter>.

MIC-3325 User Manual



Pin Assignments

This appendix describes pin assignments.

A.1 J1 Connector

Table A.1: J1 CompactPCI I/O								
Pin	Z	Α	В	С	D	E	F	
25	GND	5 V	REQ64#	ENUM#	3.3 V	5 V	GND	
24	GND	AD(1)	5 V	V(I/O)	AD(O)	ACK64#	GND	
23	GND	3.3 V	AD(4)	AD(3)	5 V	AD(2)	GND	
22	GND	AD(7)	GND	3.3 V	AD(6)	AD(5)	GND	
21	GND	3.3 V	AD(9)	AD(8)	M66EN ⁽³⁾	C/BE(0)#	GND	
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND	
19	GND	3.3 V	AD(15)	AD(14)	GND	AD(13)	GND	
18	GND	SERR#	GND	3.3 V	PAR	C/BE(1)#	GND	
17	GND	3.3 V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3 V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12-14			KI	EY AREA				
11	GND	AD(18)	AD(17)	AD(16)	GND	C/BE(2)#	GND	
10	GND	AD(21)	GND	3.3 V	AD(20)	AD(19)	GND	
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND	
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND	
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND	
6	GND	REQ0#	PRESENT#	3.3 V	CLK0	AD(31)	GND	
5	GND	NC	NC	RST#	GND	GNT0#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5 V	INTD#	GND	
2	GND	NC	5V	NC	NC	NC	GND	
1	GND	5 V	12 V	NC	12 V	5 V	GND	
Pin	Z	А	В	С	D	E	F	

Note!

NC: No Connect

#: Active Low

A.2 J2 Connector

Tab	Table A.2: J2 CompactPCI I/O								
PIN	Z	Α	В	С	D	E	F		
22	GND	GA4	GA3	GA2	GA1	GA0	GND		
21	GND	CLK6	GND	NC	NC	REAR_DET#	GND		
20	GND	CLK5	GND	NC	NC	NC	GND		
19	GND	GND	GND	reserve	reserve	reserve	GND		
18	GND	NC	NC	NC	GND	+3.3V	GND		
17	GND	NC	GND	PRST#	REQ6#	GNT6#	GND		
16	GND	GPIO0	USB6_P	DEG#	GND	NC	GND		
15	GND	VGA_B	USB6_N	FAL#	REQ5#	GNT5#	GND		
14	GND	GPIO1	USB6_OC#	USB5_OC#	SATA_TX2_N	COM3_RI#	GND		
13	GND	LAN3_TXDP0	GND	SATA_TX2_P	COM3_DTR#	COM3_CTS#	GND		
12	GND	GPIO2	LAN3_TXDN0	USB5_P	SATA_RX2_N	COM3_SOUT	GND		
11	GND	LAN3_TXDP1	GND	SATA_RX2_P	COM3_RTS#	COM3_SIN	GND		
10	GND	GPIO3	LAN3_TXDN1	USB5_N	GND	COM3_DSR#	GND		
9	GND	VGA_VS	GND	VGA_G	COM3_DCD#	COM4_RI#	GND		
8	GND	VGA_HS	LAN3_TXDP2	LAN3_TXDN2	GND	COM4_DTR#	GND		
7	GND	VGA_R	GND	+5 V	COM4_CTS#	COM4_SOUT	GND		
6	GND	VGA_DCLK	LAN3_TXDP3	LAN3_TXDN3	GND	COM4_RTS#	GND		
5	GND	VGA_DDAT	GND	SATA_TX3_N	COM4_SIN	COM4_DSR#	GND		
4	GND	V(I/O)	SATA_RX3_P	SATA_RX3_N	SATA_TX3_P	COM4_DCD#	GND		
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND		
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND		
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND		
PIN	Z	Α	В	С	D	E	F		

Note! NC: No Connect

#: Active Low

A.3 Other Connector

Ta	ble A.3: XTM B	oar	d Connector				
1	RI#	2	+12 V_XTM	3	DCD#	4	
5	SOUT	6	GND	7	SIN	8	ACZ_BITCLK
9	DTR#	10	ACZ_SYNC	11	RTS#	12	ACZ_RST#
13	DSR#	14	ACZ_SDIN0	15	CTS#	16	ACZ_SDOUT
17	GND	18	GND	19	SATA_RX2_P	20	SATA_TX2_P
21	SATA_RX2_N	22	SATA_TX2_N	23	GND	24	GND
25	USB2_P	26	USB3_P	27	USB2_N	28	USB3_N
29	GND	30	GND	31	USB2_OC#	32	KB_CLK
33	USB3_OC#	34	KB_DAT	35	PS#	36	MS_CLK
37	+5 V_XTM	38	MS_DAT	39	+5 V_XTM	40	+3.3 V_XTM
41	+5 V_XTM	42	+3.3 V_XTM	43	GND	44	+3.3 V_XTM
45	PCIE_RX0_P	46	GND	47	PCIE_RX0_N	48	PCIE_TX0_P
49	GND	50	PCIE_TX0_N	51	PCIE_RX1_P	52	GND
53	PCIE_RX1_N	54	PCIE_TX1_P	55	GND	56	PCIE_TX1_N
57	PCIE_CLK_P	58	GND	59	PCIE_CLK_N	60	TMDS_CLK_P
61	GND	62	TMDS_CLK_N	63	TMDS_DATA2_P	64	GND
65	TMDS_DATA2_N	66	TMDS_DATA1_P	67	GND	68	TMDS_DATA1_N
69	TMDS_DATA0_P	70	GND	71	TMDS_DATA0_N	72	DDC_CLK
73	GND	74	DDC_DAT	75	HPD#	76	GND
77	Control/RST#	78	I2C_CLK	79		80	I2C_DAT



Figure A.1 RJ45 LAN indicator



CPLD

This appendix describes CPLD configuration.

B.1 B.1 Features

- Hot-Swap: Hot insertion and removal control
- CompactPCI Backplane: CompactPCI slot Addressing
- LPC Bus: Provide LPC Bus access
- Watchdog: Generates a reset signal or interrupt signal when timer overflows
- Debug Message: Boot time POST message

B.2 CPLD Introduction

Advantech MIC-3325 CPLD incorporates a LPC Unit to interconnect with a controller hub of an Intel south bridge (ICH8M). The LPC Unit translates the LPC interface signals to MIC-3325 CPLD internal local bus. The CPLD Internal Local Bus is used to control and communicate with I/O space. The I/O space includes a Watch Dog unit, a debug port unit, and a cPCI slot addressing unit. In addition, there is a Hot-Swap Out-Of-Service LED control unit.

B.3 Watchdog Timer

To program the watchdog timer, you must write a program which writes a value to I/O port address 443 (hex). Any non-zero value in I/O port 443h enables the watchdog function. The watchdog reset time is $1 \sim 255$ seconds (1 second per step). Reading I/O port 444h will disable the watchdog. The return value is meaningless.



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