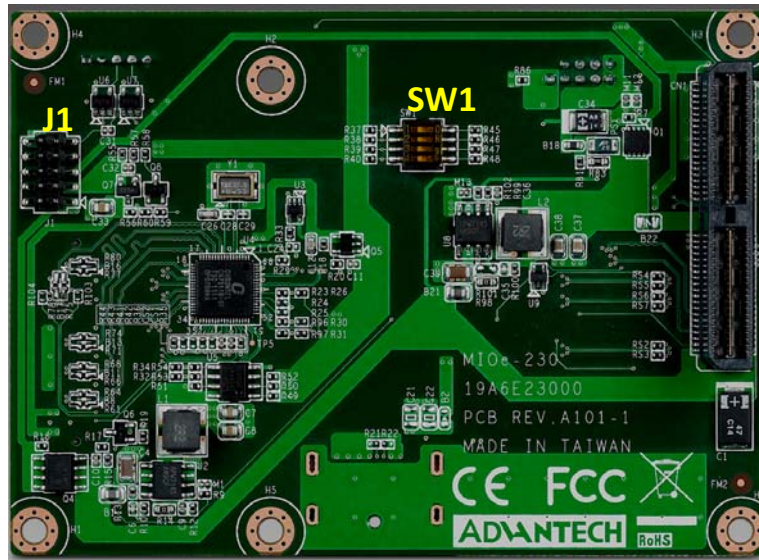


# MIOe-230 User Guide

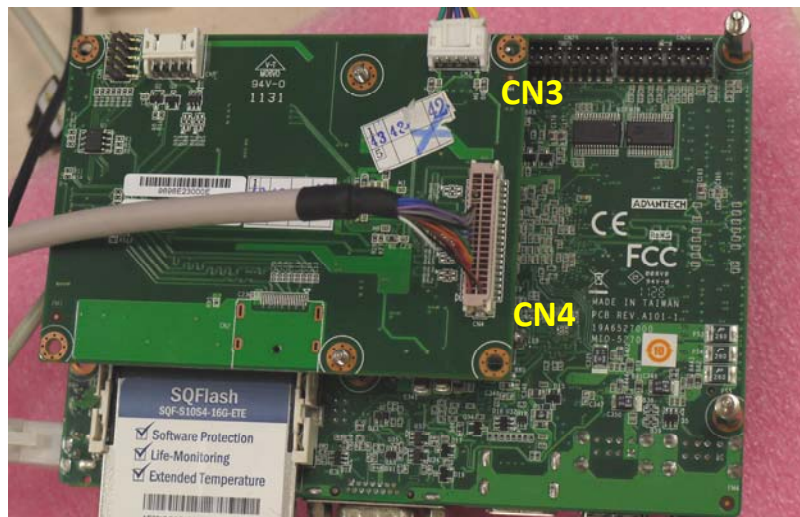
- 1.Assemble and configuration SOP
- 2.Jumper setting
- 3.Connector table
- 4.Update eeprom SOP

# Assemble and configuration SOP

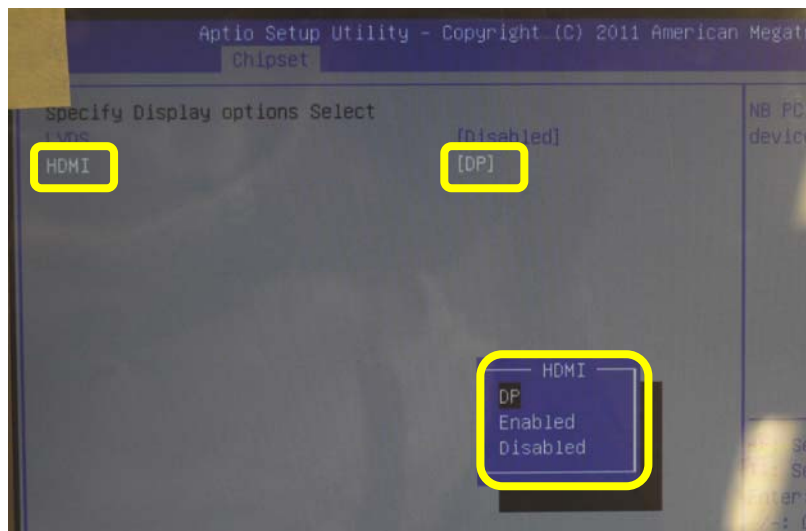
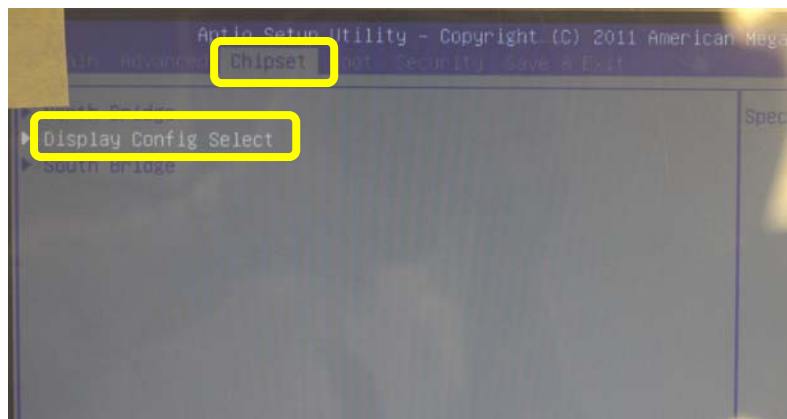
1. Choose the panel resolution and drive voltage by adjustment the **SW1** and **J1** as jumper setting document.



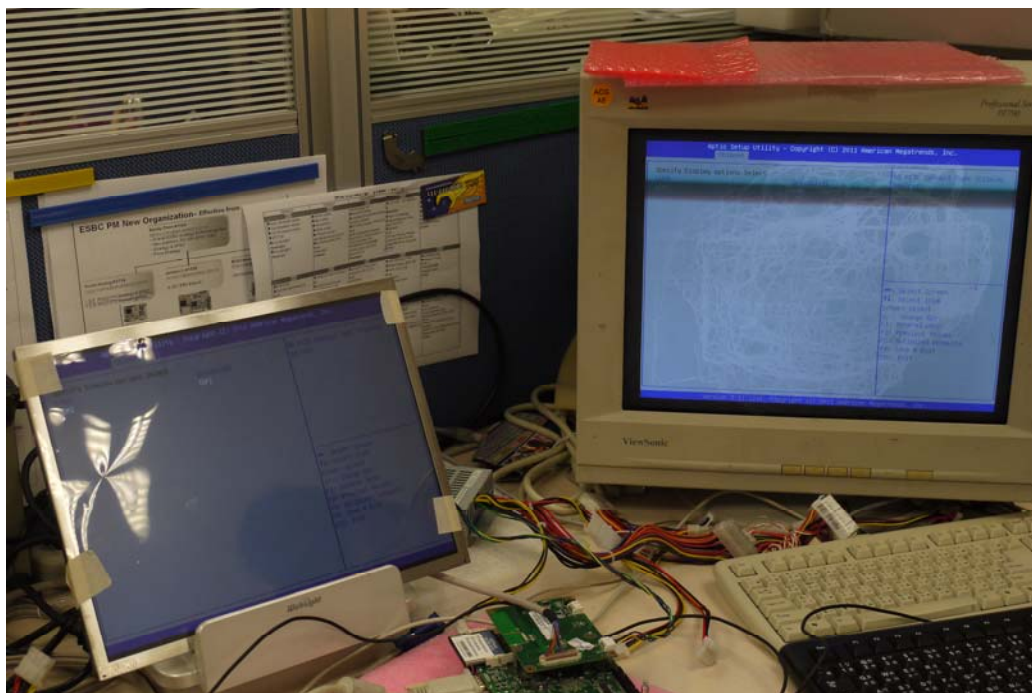
2. Assemble **MIOe-230** and **MIO-5270**.
3. Connect LVDS data signal cable to **CN4**, backlight cable to **CN3**.



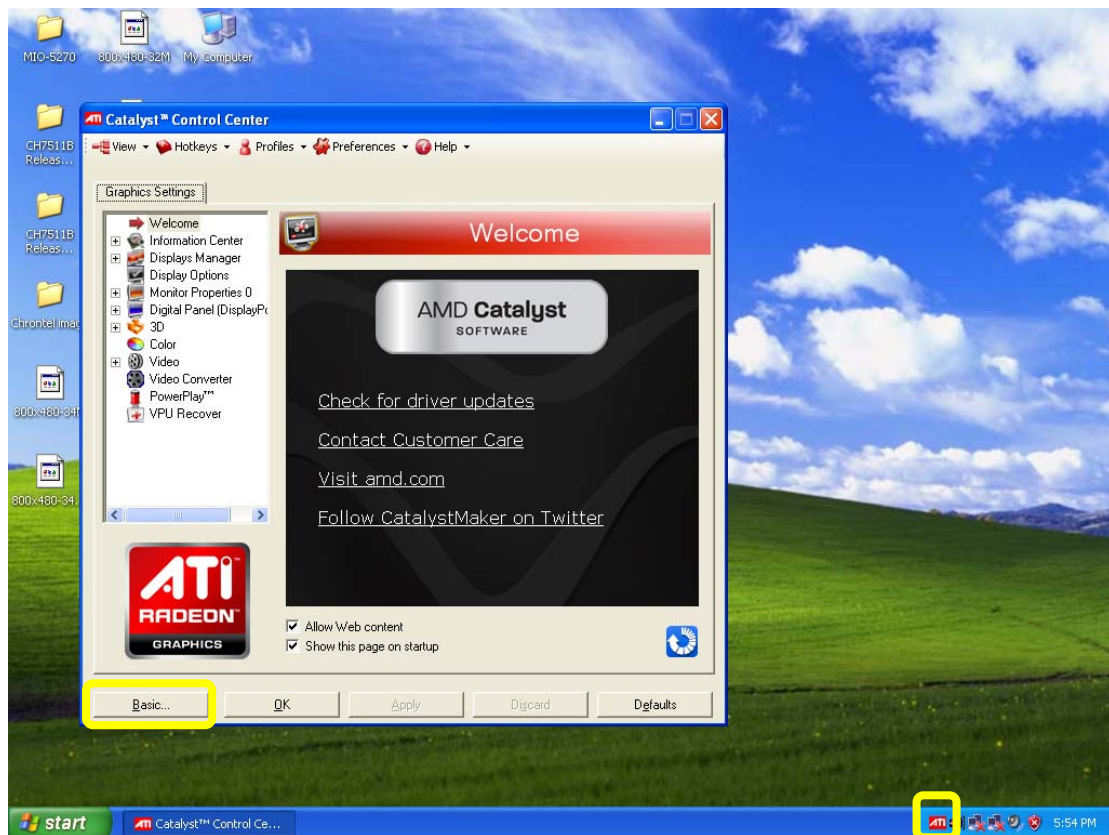
4. Check the setting in **CHIPSET**→**Display Config Select**→**HDMI**→**DP**.



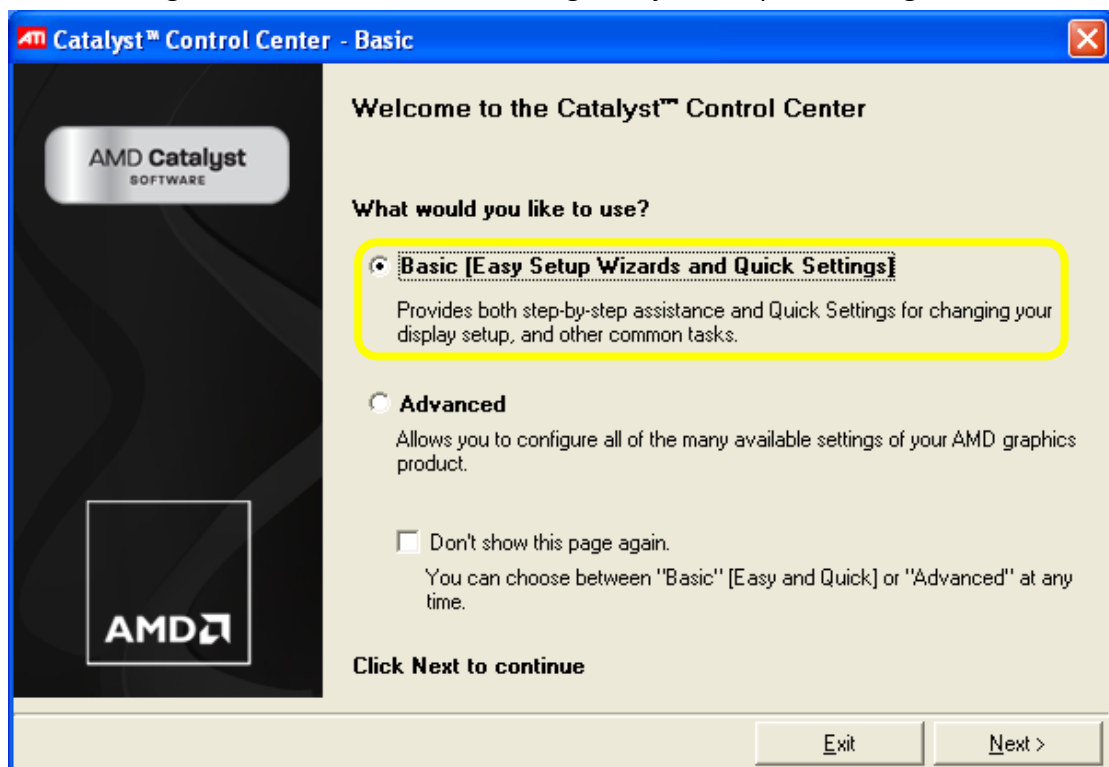
5. If all the setting is the same as above, reboot the system to check does VGA and LVDS have display at the same time. And check the resolution is match with SW1 setting.



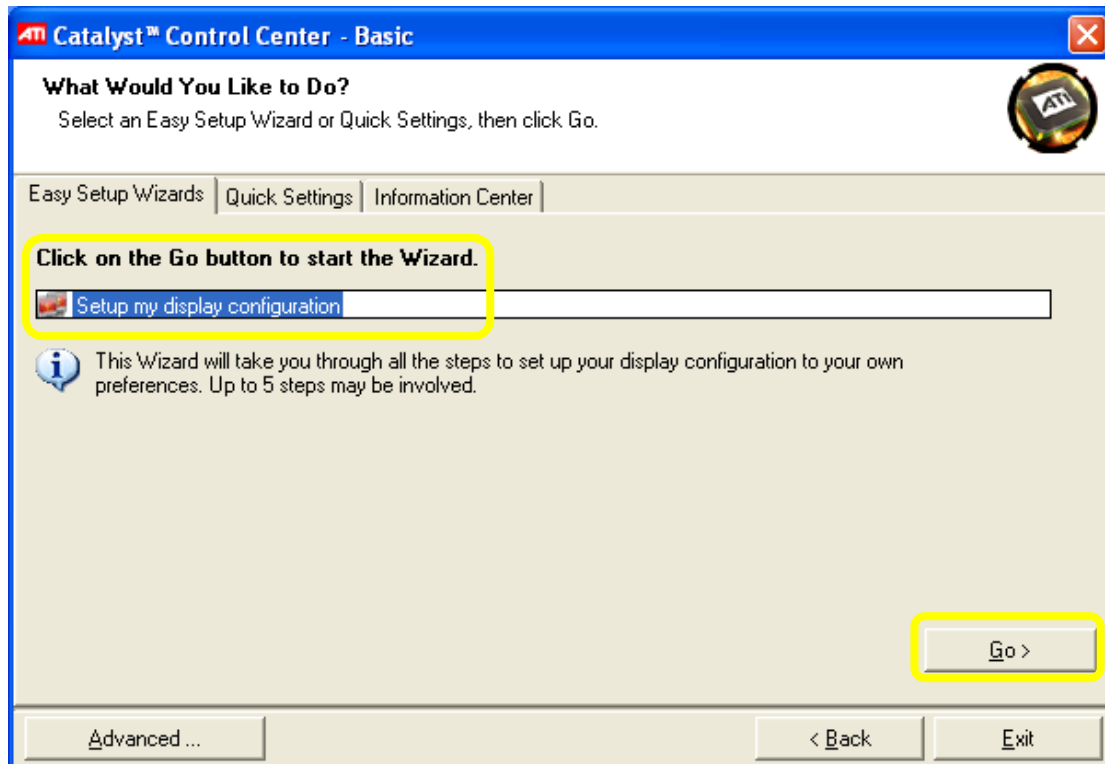
6. After entering the Windows, double click the ATI icon on toolbar to launch **Catalyst™ Control Center**, and go with basic mode.



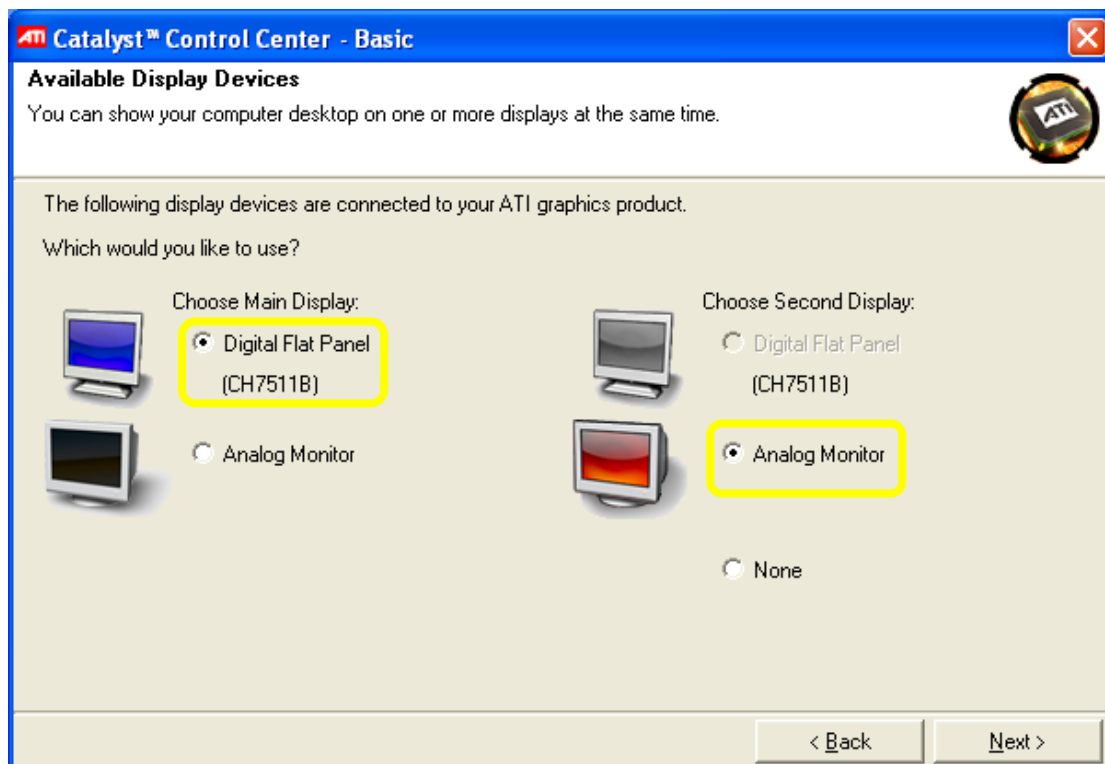
7. Following the instruction of basic setting to adjust the panel configuration.



8. Type configuration name as customize and click **Go**.

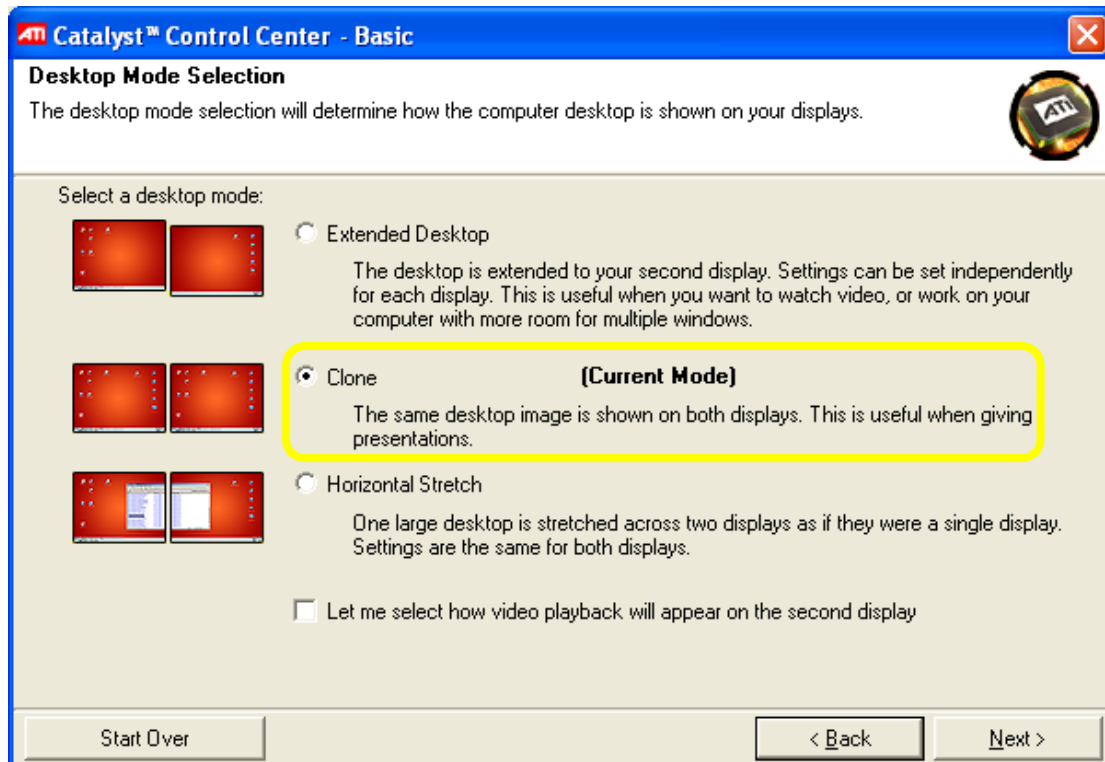


9. Choose the display device as attached.

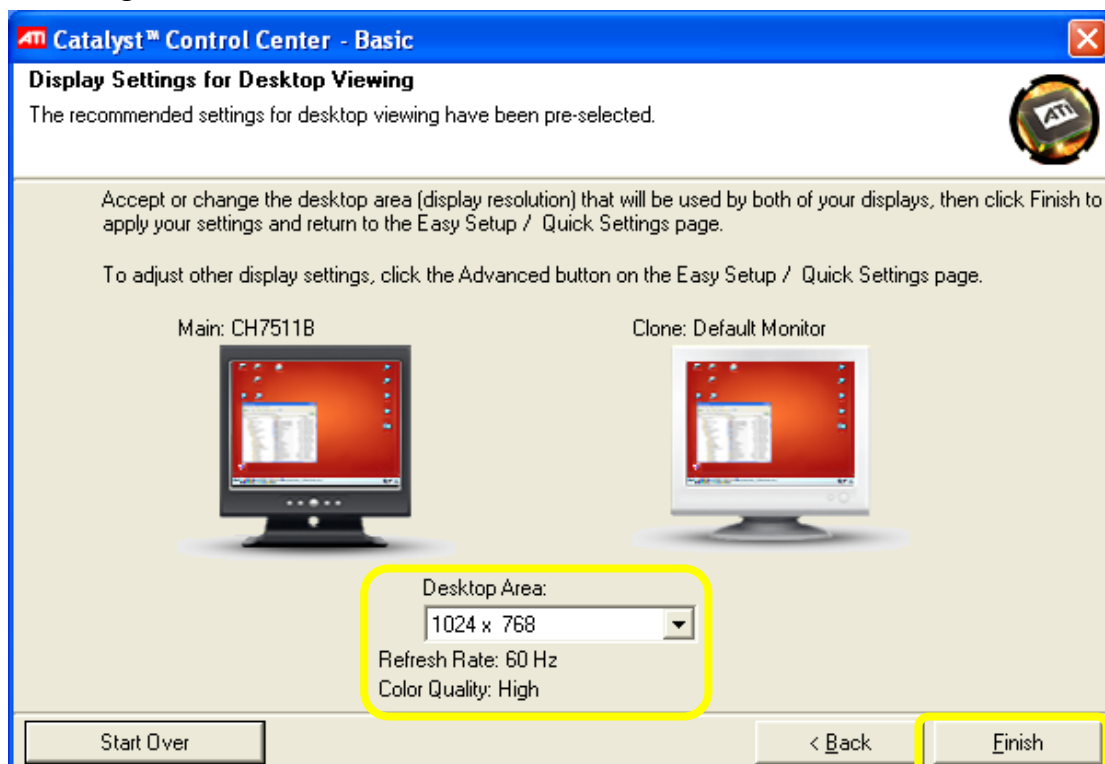


10. Choose the desktop mode as application requirement.





11. Select the resolution as application requirement and click finish to complete the configuration.

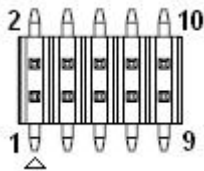


# Jumper setting

J1 Panel Voltage Sel

SW1 Panel type Sel

J1	Panel Voltage Sel
Part Number	1653005261
Footprint	HD_5x2P_79
Description	PIN HEADER 5x2P 2.0mm 180D(M) SMD 21N22050
Setting	Function
(1-3)*	+3.3V
(3-5)	+5V
(3-4)	+12V
Setting	Function
(9-10)*	Level VBR
(NL)	PWM VBR



[Home](#)

SW1	Panel type Sel
Part Number	1600000402
Footprint	SW_4x2P_50_260x315
Description	DIP SW SMD 8P SPST P=1.27mm W=5.4mm KHS42E

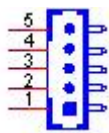
4	3	2	1	
on	on	on	on	G0 / 1.(800x480/LVDS/18bit) /WAIT , Chrontel under help
on	on	on	off	G1 / 2.(640X480/LVDS/18bits) /WAIT , no inverter to test
on	on	off	On	G2 / 3.800x600 (18bit) /DE
on	on	off	Off	G3 / 4.(1024X600/LVDS/18bits) /DE ,CK-54.2M
on	off	on	On	G4 / 5.(1024x768/LVDS/18bit ) /DE
on	off	on	Off	G5 / 6.(1280X800/LVDS/18bits) /DE
on	off	off	On	G6 / 7.(1280x1024/LVDS/48bit) /DE , CK-89M
on	off	off	Off	G7 / 8.(1366X768/LVDS/24bits) /DE , CK-80M
off	on	on	On	G8 / 9.(1440x900/LVDS/48bit) /DE
off	on	on	Off	G9 / 10.(1600x1200/LVDS/48bit) /DE , CK 162M/HB 380/VB 423



# Connector table

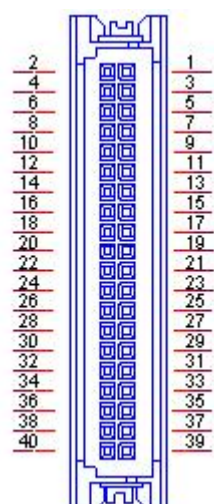
- CN3      Inverter Conn
- CN4      48 bits LVDS Panel
- CN5      USB Conn

CN3                      Inverter Conn	
Part Number	1655305120
Footprint	WHL5H-2M
Description	WAFER BOX 2.0mm 5P 90D(M) W/LOCK (2001-WR-5-LF)
Pin	Pin Name
1	+12V
2	GND
3	ENABKL
4	VBR
5	+5V



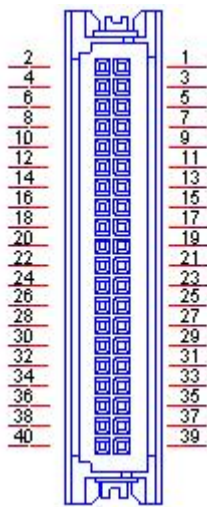
[Home](#)

<b>CN4</b>	<b>48 bits LVDS Panel</b>
<b>Part Number</b>	1653920200
<b>Footprint</b>	SPH20X2
<b>Description</b>	*CONN. DF13-40DP-1.25V
<b>Pin</b>	<b>Pin Name</b>
1	+5V or +3.3V
2	+5V or +3.3V
3	GND
4	GND
5	+5V or +3.3V
6	+5V or +3.3V
7	LVDS0_D0-
8	LVDS1_D0-
9	LVDS0_D0+
10	LVDS1_D0+
11	GND
12	GND
13	LVDS0_D1-
14	LVDS1_D1-
15	LVDS0_D1+
16	LVDS1_D1+
17	GND
18	GND
19	LVDS0_D2-
20	LVDS1_D2-
21	LVDS0_D2+
22	LVDS1_D2+
23	GND
24	GND
25	LVDS0_CLK-
26	LVDS1_CLK-



[Home](#)

CN4	48 bits LVDS Panel
Part Number	1653920200
Footprint	SPH20X2
Description	*CONN. DF13-40DP-1.25V
Pin	Pin Name
27	LVDS0_CLK+
28	LVDS1_CLK+
29	GND
30	GND
31	NC
32	NC
33	GND
34	GND
35	LVDS0_D3-
36	LVDS1_D3-
37	LVDS0_D3+
38	LVDS1_D3+
39	NC
40	NC

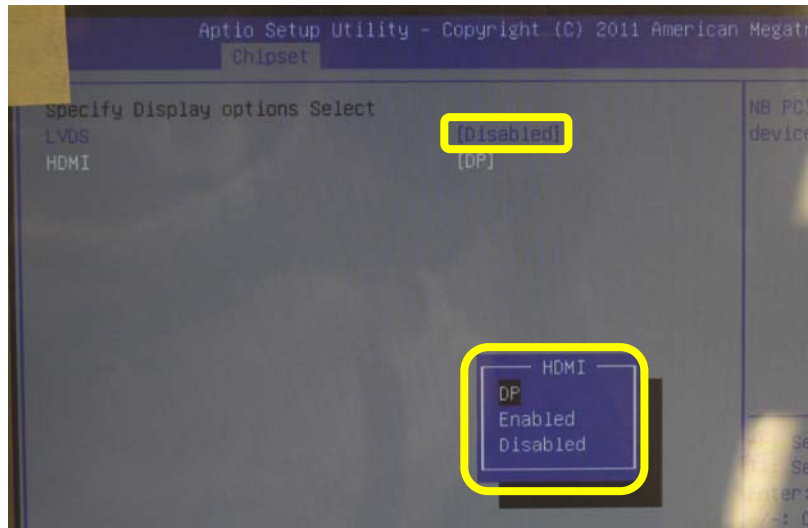


CN5	USB Conn
Part Number	1655003991
Footprint	WF_5x2P_79_BOX_RA_N2_D
Description	
Pin	Pin Name
1	GND_USB
2	N/A
3	GND
4	GND
5	USB0_P+
6	USB1_P+
7	USB0_P-
8	USB0_P+
9	+V5_USB
10	+V5_USB

[Home](#)

# Update eeprom SOP

1. Check the setting in **CHIPSET**→**Display Config Select**→**HDMI**→**DP**, and ensure **LVDS** has been set to **Disabled**



2. The other procedure can refer to **Customize the EEPROM for Chrontel chip on MIO-series & MIOe-series** document from ECG AE. It will update the eeprom on MIOe-230 instead of MIO-5270's.